ANALOG CIRCUITS LAB MANUAL

Department of Electronics & Communication Engineering

VEMU INSTITUTE OF TECHNOLOGY::P.KOTHAKOTA

NEAR PAKALA, CHITTOOR-517112

(Approved by AICTE, New Delhi & Affiliated to JNTUA, Anantapuramu)

ANALOG CIRCUITS LAB MANUAL

Name:____

H.T.No:____

Year/Semester:______________________________________

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VEMU Institute of Technology
Dept. of Electronics and Communication Engineering

Vision of the institute

To be one of the premier institutes for professional education producing dynamic and vibrant force of technocrats with competent skills, innovative ideas and leadership qualities to serve the society with ethical and benevolent approach.

Mission of the institute

Mission_1: To create a learning environment with state-of-the art infrastructure, well equipped laboratories, research facilities and qualified senior faculty to impart high quality technical education.
Mission_2: To facilitate the learners to inculcate competent research skills and innovative ideas by Industry-Institute Interaction.
Mission_3: To develop hard work, honesty, leadership qualities and sense of direction in learners by providing value based education.

Vision of the department

To develop as a center of excellence in the Electronics and Communication Engineering field and produce graduates with Technical Skills, Competency, Quality, and Professional Ethics to meet the challenges of the Industry and evolving Society.

Mission of the department

Mission_1: To enrich Technical Skills of students through Effective Teaching and Learning practices to exchange ideas and dissemination of knowledge.

Mission_2: To enable students to develop skill sets through adequate facilities, training on core and multidisciplinary technologies and Competency Enhancement Programs.

Mission_3: To provide training, instill creative thinking and research attitude to the students through Industry-Institute Interaction along with Professional Ethics and values.

Programme Educational Objectives (PEOs)

PEO 1: To prepare the graduates to be able to plan, analyze and provide innovative ideas to investigate complex engineering problems of industry in the field of Electronics and Communication Engineering using contemporary design and simulation tools.

PEO-2: To provide students with solid fundamentals in core and multidisciplinary domain for successful implementation of engineering products and also to pursue higher studies.

PEO-3: To inculcate learners with professional and ethical attitude, effective communication skills, teamwork skills, and an ability to relate engineering issues to broader social context at work place

Programme Outcomes(Pos)

PO_1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO_2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO_3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO_4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO_5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO_6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO_7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO_8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO_9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO_10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO_11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO_12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Programme Specific Outcome(PSOs)

PSO_1	**Higher Education :** Qualify in competitive examination for pursuing higher education by applying the fundamental concepts of Electronics and Communication Engineering domains such as Analog & Digital Electronics, Signal Processing, Communication & Networking, Embeded Systems, VLSI Design and Control systems etc.,
PSO_2	**Employment**: Get employed in allied industries through their proficiency in program specific domain knowledge, Specalized software packages and Computer programming or became an entrepreneur.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

II B.Tech. I-Sem (ECE)

(20A04302P) ANALOG CIRCUITS LABORATORY

COURSE OUTCOMES(CO_S)

CO No.	Description	Blooms Level
C229.1	Understand the Characteristics and Frequency response of various amplifiers	2
C229.2	Analyze and Design negative Feedback amplifiers, Oscillators and Tuned amplifiers.	4
C229.3	Determine the efficiency of various Power Amplifiers	2

LIST OF EXPERIMENTS:

1. Design and Analysis of Darlington pair.
2. Frequency response of CE – CC multistage Amplifier
3. Design and Analysis of Cascode Amplifier.
4. Frequency Response of Differential Amplifier
5. Design and Analysis of Series – Series feedback amplifier and find the frequency response of it.
6. Design and Analysis of Shunt – Shunt feedback amplifier and find the frequency response of it.
7. Design and Analysis of Class A power amplifier
8. Design and Analysis of Class AB amplifier
9. Design and Analysis of RC phase shift oscillator
10. Design and Analysis of LC Oscillator
11. Frequency Response of Single Tuned amplifier
12. Design and Analysis of Bistable Multivibrator
13. Design and Analysis of Monostable Multivibrator
14. Design and Analysis of Astable Multivibrator

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Dept. of Electronics and Communication Engineering

(20A04302P) ANALOG CIRCUITS LABORATORY II B.Tech. I-Sem LIST OF EXPERIMENTS TO BE CONDUCTED

1. Design and Analysis of Darlington pair.
2. Design and Analysis of Cascode Amplifier.
3. Frequency Response of Differential Amplifier
4. Design and Analysis of Series – Series feedback amplifier and find the frequency response of it.
5. Design and Analysis of Shunt – Shunt feedback amplifier and find the frequency response of it.
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7. Design and Analysis of RC phase shift oscillator
8. Design and Analysis of LC Oscillator
9. Frequency Response of Single Tuned amplifier
10. Design and Analysis of Bistable Multivibrator
11. Design and Analysis of Monostable Multivibrator
12. Design and Analysis of Astable Multivibrator

ADVANCED EXPERIMENTS:

1. Class B Push Pull Power Amplifier
2. Cascade Amplifier

CONTENTS

DOS & DONTS IN LABORATORY

DO’s

1. Students should be punctual and regular to the laboratory.
2. Students should come to the lab in-time with proper dress code.
3. Students should maintain discipline all the time and obey the instructions.
4. Students should carry observation and record completed in all aspects.
5. Students should be at their concerned experiment table, unnecessary moment is restricted.
6. Students should follow the indent procedure to receive and deposit the components from lab technician.
7. While doing the experiments any failure/malfunction must be reported to the faculty.
8. Students should check the connections of circuit properly before switch ON the power supply.
9. Students should verify the reading with the help of the lab instructor after completion of experiment.
10. Students must endure that all switches are in the lab OFF position, all the connections are removed.
11. At the end of practical class the apparatus should be returned to the lab technician and take back the indent slip.
12. After completing your lab session SHUTDOWN the systems, TURNOFF the power switches and arrange the chairs properly.
13. Each experiment should be written in the record note book only after getting signature from the lab in charge in the observation notebook.

DON’Ts

1. Don’t eat and drink in the laboratory.
2. Don’t touch electric wires.
3. Don’t turn ON the circuit unless it is completed.
4. Avoid making loose connections.
5. Don’t leave the lab without permission.
6. Don’t bring mobiles into laboratory.
7. Do not open any irrelevant sites on computer.
8. Don’t use a flash drive on computers.

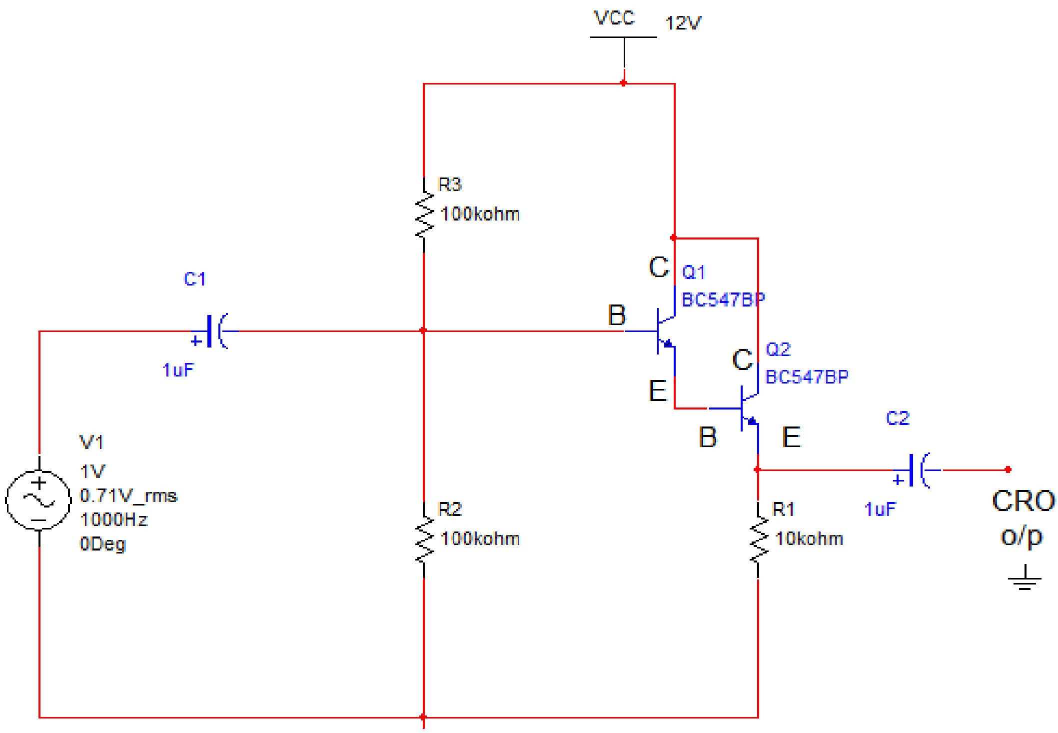
SCHEME OF EVALUATION

S.No	Program	Date	Marks Awarded				Total 30(M)
			Record (10M)	Obs. (10M)	Viva (5M)	Attd. (5M)	
1	Design and Analysis of Darlington pair.						
2	Design and Analysis of Cascode Amplifier.						
3	Frequency Response of Differential Amplifier						
4	Design and Analysis of Series – Series feedback amplifier						
5	Design and Analysis of Shunt – Shunt feedback amplifier						
6	Design and Analysis of Class A power amplifier						
7	Design and Analysis of RC phase shift oscillator						
8	Design and Analysis of LC Oscillator						
9	Frequency Response of Single Tuned amplifier						
10	Design and Analysis of Bitable Multivibrator						
11	Design and Analysis of Monostable Multivibrator						
12	Design and Analysis of Astable Multivibrator						
ADVANCED EXPERIMENTS							
1	Class B Push Pull Power Amplifier						
2	Cascade Amplifier						

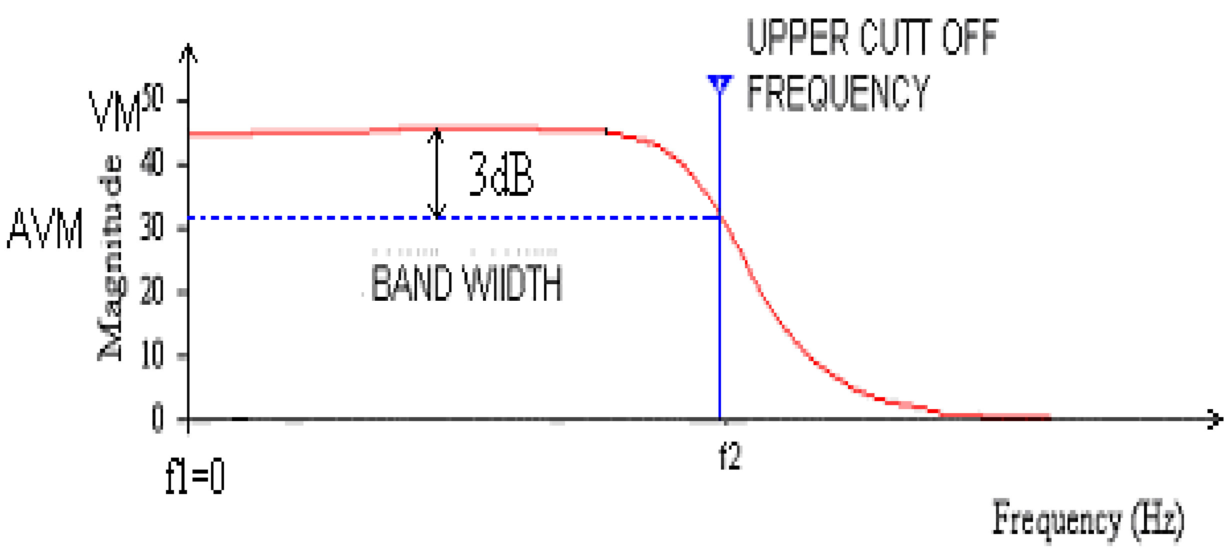
Signature of Lab In-charge

CIRCUIT DIAGRAM:

Darlington Pair



MODEL WAVE FORM:



Exp No:01 **Date:**

DARLINGTON PAIR

AIM: To design and construct a Darlington amplifier and to calculate the bandwidth and cut off Frequency.

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	Transistor	BC -547	2
2	Resistors	100KΩ, 10KΩ	2
3	Capacitors	1uf	2
4	Function Generator	0-3MHz	1
5	RPS	0-30V	1
6	CRO	0-30MHz	1
7	Bread Board	-	1
8	Connecting Wires	-	As Per Required

OPERATION:

A Darlington transistor pair comprises of a couple of bipolar transistors that are coupled in order to deliver a very high-current gain from a low-base current. It is cascading of common collector-common collector. In this circuit, the emitter of the input transistor is connected to the base terminal of the output transistor. Therefore, the current that is amplified by the first transistor is again amplified by the second transistor. The current gain of single stage cc amplifier is high, so by using Darlington pair we can get high current gain.

PROCEDURE:

1. Design the circuit for given specifications and connect the circuit.
2. Apply input signal to the circuit of $2V_{p-p}$, 1 KHz sine wave from the function generator with DC offset ON.
3. Tabulate amplitude of output signal with change in frequency with steps from 10Hz to 1MHz and determine gain using $A_v = V_0/V_s$.
4. Calculate voltage gain in dB using $A_v = 20 \log_{10}(V_0/V_s)$.
5. Plot the frequency response on semi-log graph using the values of amplitude in dB Vs frequency in Hz.
6. Calculate the bandwidth using $BW = f_2 – f_1$

DESIGN OF DARLINGTON AMPLIFIER

Design parameters

Vcc=12V, Ie=2mA, h_{fe} (β) =100, Vbe =0.7V,

S=10,

Load resistance, R_L=4.7 kΩ

Design specifications

Vcc – V_{CE}-V_E =0

V_{CE} =50% of Vcc

V_{CE} =0.5 * 12 =6 V

V_E=12- 6

V_E=6V

To find R_{eff} $V_E = I_E \times R_{eff}$ $R_{eff} = V_E / I_E$

R_{eff} = 6 / 2x10-3

R_{eff}= 3 KΩ

To find R_E $R_{eff} = R_E \parallel R_L$

3 KΩ = R_E*4.7KΩ / R_E+4.7KΩ

R_E = 8.2 KΩ use approx 10 KΩ

For determining the values of R_1 & R_2 ($R_B = R_1 \parallel R_2$) following steps should be followed

Step 1 : Calculate R_B

Step 2 : Calculate V_{TH}

Let

$R_B = R_1 \parallel R_2$

$R_B = R_1 * R_2 / R_1 + R_2$----------------- (1)

V_{TH}= Vcc*R_2 / R_1+R_2--------------- (2)

Calculation of R_B From Approx analysis S = 1+ (R_B / R_E)

10 = 1 + R_B / 8.2 KΩ

9*8.2 KΩ = R_B R_B =73 KΩ

Calculation of V_{TH} $V_{TH} – V_{BE} – V_E$ =0 $V_{TH} = V_{BE} + V_E$ V_{TH} = 0.7 + 6

V_{TH} = 6.7 V

From eqn (2)

V_{TH} / Vcc = R_2 / R_1+R_2 6.7 / 12 = R_2 / R_1+R_2

0.558 = R_2 / R_1+R_2----------------- (3)

To find R_1

From (1)

$R_B = R_1 * R_2 / R_1 + R_2$ 7300 = 0.558 * R_1

R_1 = 130 kΩ use approx 150 kΩ

To find R_2

From (3)

0.558 = R_2 / R_1+R_2 0.558 (R_1+R_2) = R_2

0.558 (130x10^3 + R_2) = R_2

R_2 = 162 kΩ use approx 150

OBSERVATIONS:

V_i=2V

S.NO	FREQUENCY(Hz)	OUTPUT VOLTAGE (V)	GAIN (V_0/V_s)	GAIN IN dB A_v=20 $\log_{10}$ (V_0/V_s)

PRECUATIONS:

1. DC offset should be ON, to avoid clipping.

CALCULATIONS :

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. How do you calculate the overall current gain of a Darlington pair?

2. What is the gain of Darlington transistor pair?

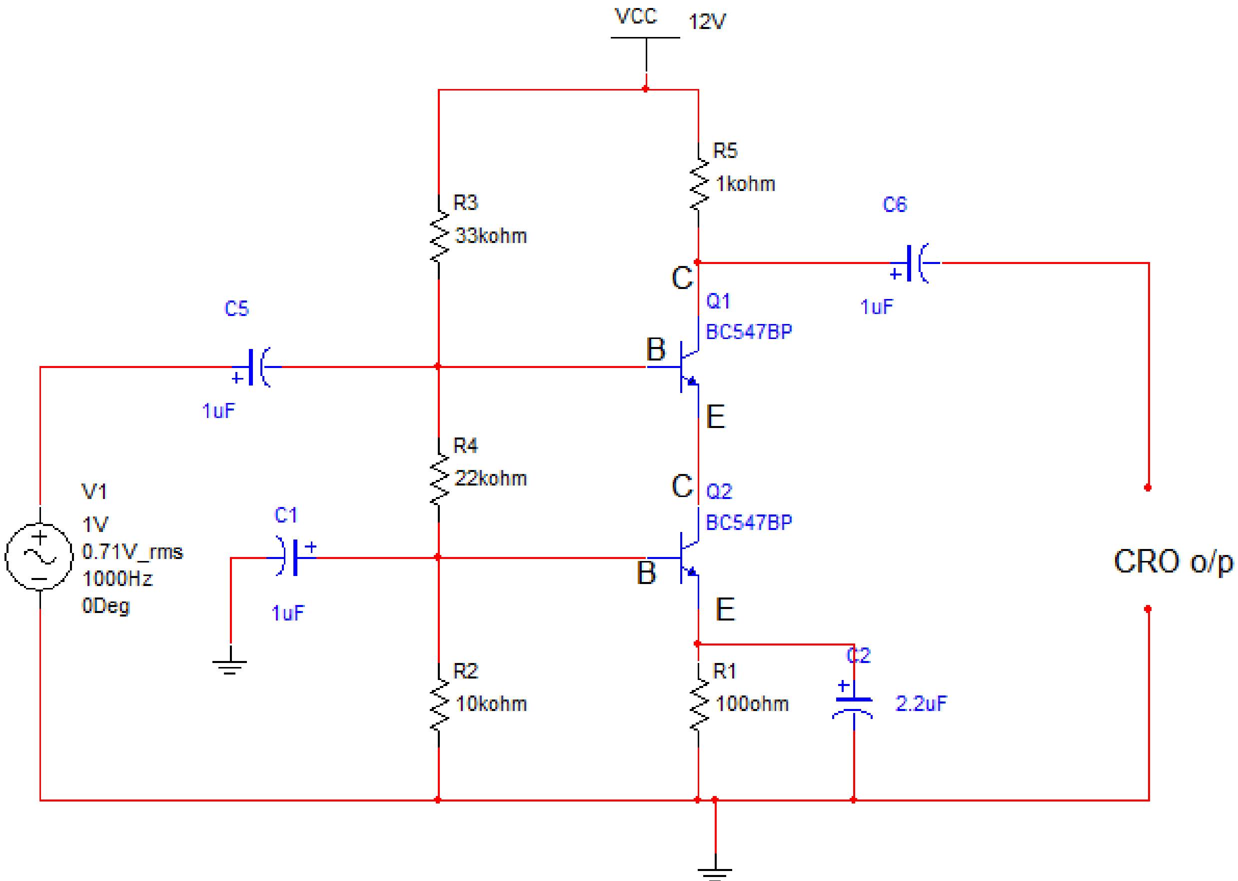
3. How do you make a Darlington pair?

4. What does a Darlington pair do?

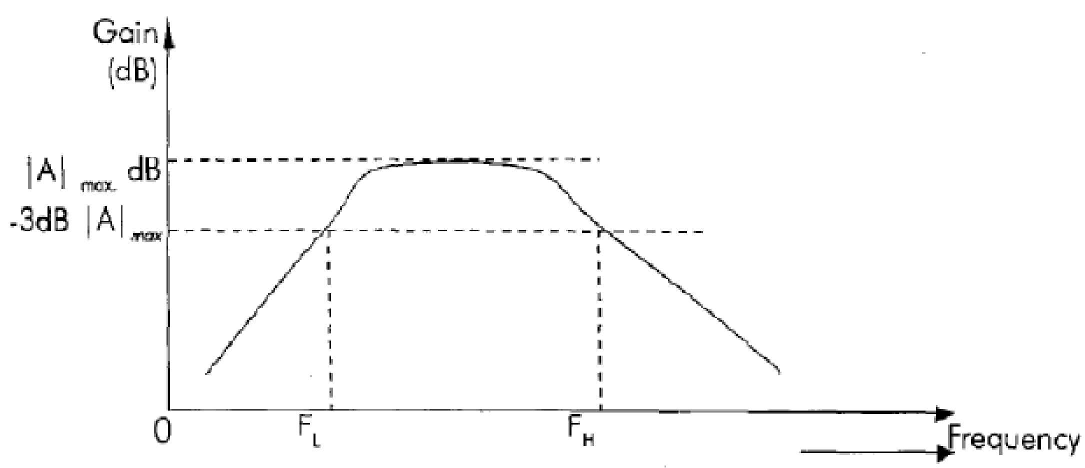
5. Why is it called emitter follower?

CIRCUIT DIAGRAM:

CASCODE AMPLIFIER:



MODEL WAVE FORM:



Bandwidth=$f_H - f_L$

Exp No:02 **Date:**

CASCODE AMPLIFIER

AIM: To design and construct a cascade amplifier circuit and to draw its frequency response graph.

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	Transistor	BC107 or BC547	2
2	Resistors	33KΩ	1
		22KΩ	1
		10KΩ	1
		1KΩ	1
		100Ω	1
3	Capacitors	1µF	2
		2.2 µF	1
4	RPS	0-30V	1
5	Function Generator	0-3MHz	1
6	CRO	30MHz	1
7	Bread board	-	1
8	Connecting wires	-	As Per Required

OPERATION:

Cascode amplifier is a two stage circuit consisting of a transconductance amplifier followed by a buffer amplifier. The word “cascade” was originated from the phrase“cascade to cathode”. This circuit have a lot of advantages over the single stage amplifier like, better input output isolation, better gain, improved bandwidth, higher input impedance, higher output impedance, better stability, higher slew rate etc. The reason behind the increase in bandwidth is the reduction of Miller effect. Cascode amplifier is generally constructed using FET (field effect transistor) or BJT (bipolar junction transistor). One stage will be usually wired in common source/common emitter mode and the other stage will be wired in common base/ common emitter mode

PRECAUTIONS

Avoid loose connections give proper input voltage

DESIGN :

Design parameters

V_{cc}=12V, I_c =2mA, h_{fe} (β) =100, V_{be} =0.7V,

V_{CE1}= V_{CE2}=35% of Vcc = 4.2V

V_{RE}=10% of V_{CC} =1.2V V_{RC}=20% of V_{CC}=2.4V

To find Rc

V_{RC} =Ic*Rc =2.4V

Rc=1.2KΩ

To find R_E

V_{RE} =I_E*R_E =1.2V R_E=600Ω

To find R_1, R_2 and R_3

Vcc-V_{R1}-V_{BE1}-V_{CE2}-V_{RE}=0 V_{R1}=Vcc-V_{BE1}-V_{CE2}-V_{RE} V_{R1}=12-0.6-4.2-12= 6V

I_B=Ic/Hfe = 20μA

If 10I_B assumed flowing through R_1 we get

R1= V_{R1}/10 I_B = 30KΩ

Vcc-V_{R1}-V_{R2}-V_{BE2}-V_{RE}=0 V_{R2}=Vcc- V_{R1} -V_{BE2}-V_{RE} V_{R2}=12- 6-0.6-1.2= 4.2V

I_B=Ic/Hfe = 20μA

If 9I_B assumed flowing through R_2 we get

R2= V_{R2}/9 I_B = 23KΩ

V_{R3}-V_{BE2}-V_{RE}=0 V_{R3}= V_{BE2}+V_{RE} V_{R3}= 0.6+1.2= 1.8V

I_B=Ic/Hfe = 20μA

If 8I_B assumed flowing through R_3 we get

R3= V_{R3}/8 I_B = 11.2KΩ

To find C_E (Bypass capacitor) X_{CE} =R_E / 10

X_{CE} = 600Ω /10 =60

X_{CE} =1 / 2π f C_E Let f=1000

C_E = 1 / 2*π *1000* 60 =2.2 μf

PROCEDURE:

1. Connect the circuit diagram as shown in figure for cascode amplifier on breadboard.
2. Adjust input signal amplitude in the function generator and observe an amplified voltage at the output without distortion.
3. By keeping input signal voltage, say at 50mV, vary the input signal frequency from 0 to 1MHz in steps as shown in tabular column and note the corresponding output voltages.
4. Find the voltage gain, A_v=20 $\log_{10}$ (V_0/V_i)
5. Plot AV VS frequency on a semi-log sheet.

OBSERVATIONS:

V_S=50mV

S.NO	FREQUENCY(Hz)	OUTPUT VOLTAGE (V)	GAIN(V_0/V_i)	GAIN IN dB A_v=20 $\log_{10}$ (V_0/V_i)

RESULT:

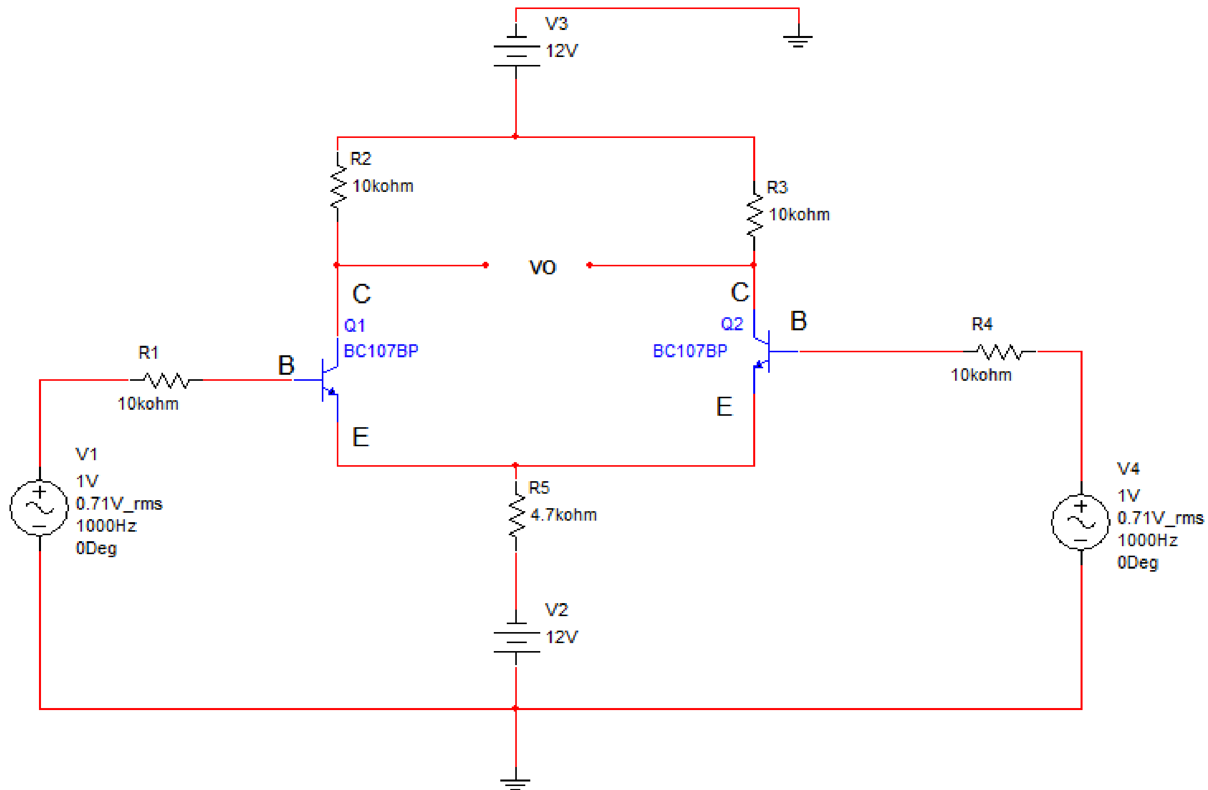
CONCLUSION:

VIVA QUESTIONS:

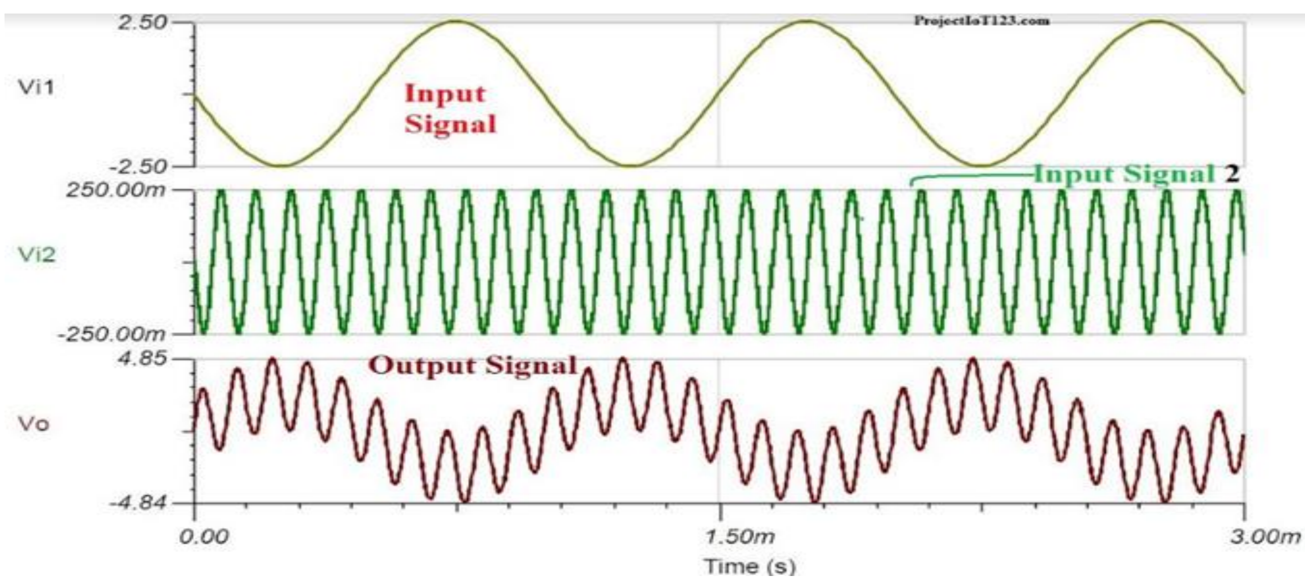
1. Why cascode amplifier is used?
2. What are the features of cascode amplifier?
3. When amplifiers are cascaded the result is?
4. What is difference between Cascade and cascode?
5. Why cascode current mirrors are used?

Circuit Diagram:

DIFFERENTIAL AMPLIFIER:



MODEL WAVE :



Exp No: 03 **DATE:**

DIFFERENTIAL AMPLIFIER

AIM: To design a differential amplifier and verify the frequency response.

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	Transistor	(BC107 or BC547)	2
2	Resistors	10K	4
		4.7K	1
3	RPS	0-12V	1
4	Function Generator	0-3MHz	1
5	CRO	30MHz	1
6	Bread board	-	1
7	Connecting wires	-	As Per Required

PROCEDURE:

1. Connections are given as per circuit diagram
2. Set Vs =50 mV, using signal generator
3. Keeping the input voltage constant vary the frequency from 50Hz to1MHz in regular steps
4. Observe both input and output on the CRO (sine wave)
5. The differential gain is calculated at mid frequency range where the magnitude of the sine wave is maximum.
6. The differential gain is calculated by Ad = Vo / Vi

RECAUTIONS:

Avoid loose connections give proper input voltage

Design Procedure:

$V_{cc}=12V$, $V_{ee} = -12V$, $I_{c_1} = I_{c_1} = 2mA$, $I_e=4mA$, h_{fe} (β) =300, V_{be} =0.7V, h_{ie} =4.7kΩ

NOTE:

Vcc =12V

V_{RE} =10% of Vcc =0.1 * 12 = 1.2 V

V_{RC} =40% of Vcc =0.4 * 12 = 4.8 V

V_{CE} =50% of Vcc =0.5 * 12 = 6 V $I_{c1} = I_{c1}$ = 2mA

To find Rc:

Apply KVL to collector loop

Vcc-IcRc-Vce-IeRe – Vee =0

Rc = {Vcc- Vce - V_{RE} - Vee }/ Ic

= {12-6 -1.2 –(-12)} /2x10^{-3}

Rc = 8.7kΩ use approx 10 kΩ

To find Re:

Apply KVL to collector loop

Vcc-IcRc-Vce-IeRe – Vee =0

Re = {Vcc- V_{RC} – Vce - Vee}/ Ie

= {12 - 4.8 – 6 – (-12)} /4x10^{-3}

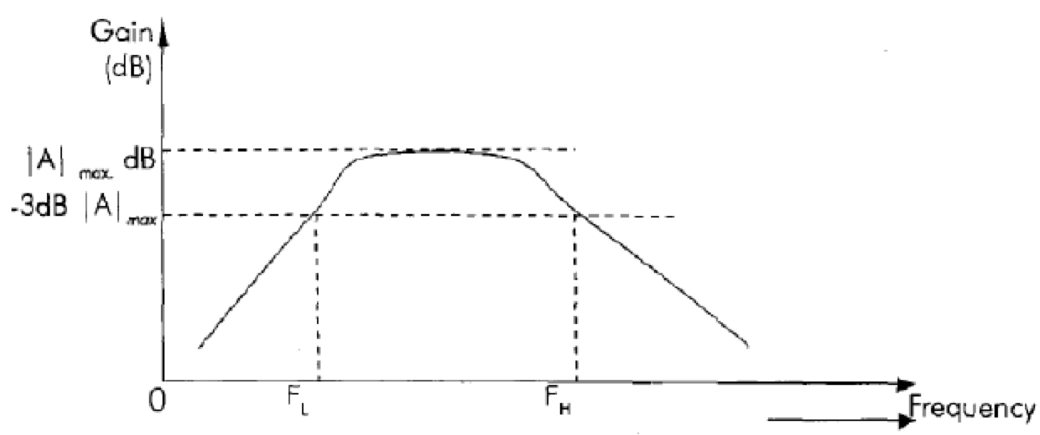
Re = 3.3 kΩ use approx 4.7k

OBSERVATIONS:

V_S=20mV

S.No	Frequency(Hz)	Output Voltage (V)	Gain=(V_0/V_i)	Gain in dB $A_v=20\log_{10}(V_0/V_i)$

MODEL GRAPH:



Bandwidth=$f_H - f_L$

RESULT:

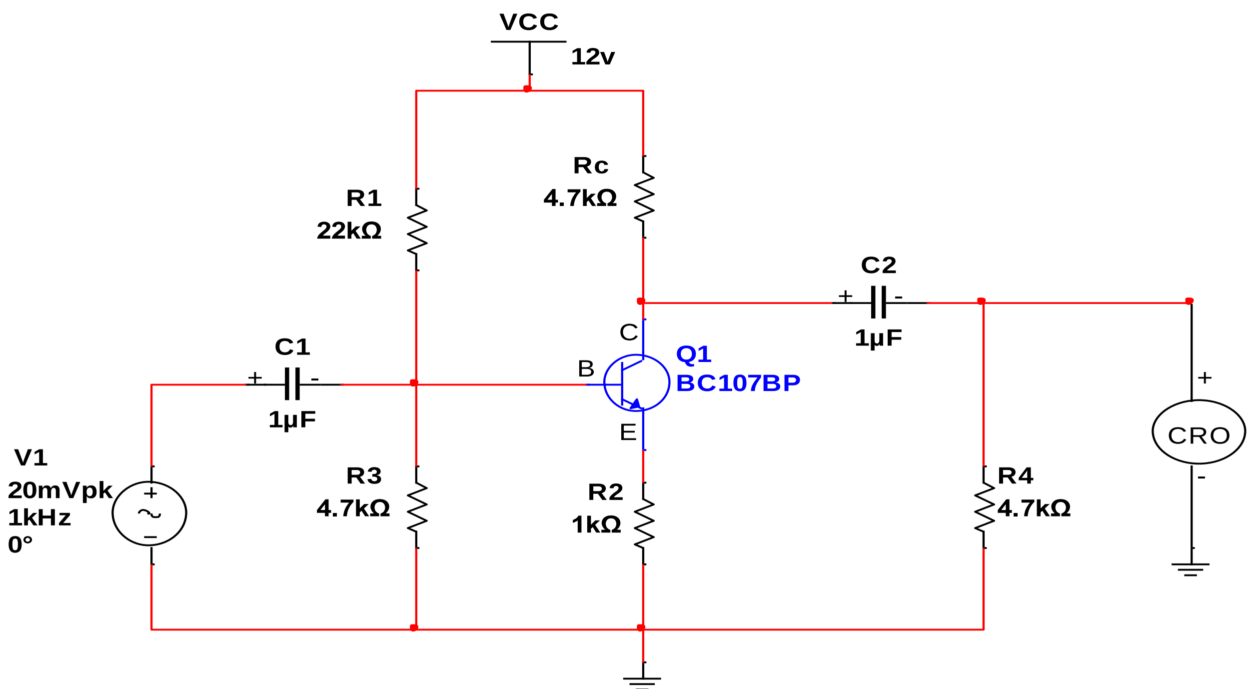
CONCLUSION:

VIVA QUESTIONS:

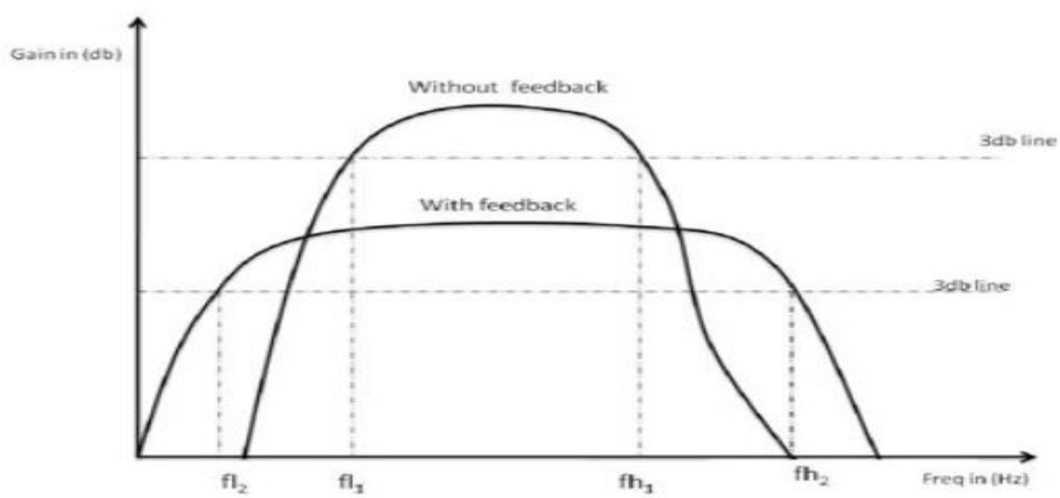
1. What is CMRR?
2. What is Amplifier?
3. What Does Differential amplifier do?
4. what are the types of differential amplifier?
5. what are the advantages of differential amplifier?

CIRCUIT DIAGRAM:

Current Series Feedback Amplifier



MODEL GRAPH:



Exp No: 04 **Date:**

CURRENT –SERIES (SERIES- SERIES) FEEDBACK AMPLIFIER

AIM: To design and test the current-series feedback amplifier and calculate the following parameters with feedback.

1. Mid band gain.

2. Bandwidth and cut-off frequencies.

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	Transistor	BC107BP	1
2	Resistors	22KΩ	1
		1KΩ	1
		4.7KΩ	3
3	Capacitors	1µF	2
4	RPS	0-30V	1
5	Function Generator	0-3MHz	1
6	CRO	30MHz	1
7	Bread board	-	1
8	Connecting wires	-	As Per Required

PROCEDURE:

1. Connect the circuit as per the circuit diagram.

2. Keeping the input voltage constant, vary the frequency from 50Hz to 3MHz in regular steps and note down the corresponding output voltage.

3. Plot the graph: Gain (dB) Vs Frequency

4. Calculate the bandwidth from the graph.

5. Calculate the input and output impedance.

6. Remove Emitter Capacitance, and follow the same procedures (1 to 5).

DESIGN PROCEDURE/ DESIGN CALCULATIONS:

V_{cc}=12v; Ic=1mA; $f_{L=}$50Hz; S=2; R_L=4.7KΩ

$r_e = \frac{26mV}{Ic}$=26Ω

$V_{ce} = \frac{Vcc}{2}$ =6V

$V_E = Vcc/10$ = 1.2V

$h_{ie} = h_{fe}\, r_e$ = 2.6KΩ

Applying KVL output loop, we get

$V_{cc} = I_E R_E + I_C R_C + V_{ce}$;

$12=1x10^{-3}xR_C+6+1.2$

R_C = 4.8 KΩ

R_L =4.7KΩ

Since I_B is very small when compare with I_C , $I_C \approx I_E$

$R_E = \frac{V_E}{I_E}$ =1.2KΩ

$S = 1+ \frac{R_B}{R_E}$

$2=1+(R_{B/1.2K)}$

R_B =1.2KΩ

$V_B = \frac{V_{CC}R_2}{R_1+R_2}$

$0.7=\frac{12R2}{R1+R2}$

$\frac{R2}{R1+R2}$=0.05

$R_B = R_1 \parallel R_2$

By substituting above equation we will get

R_1 =24KΩ,

R2=1.5kΩ

$X_{Ci} = \frac{h_{ie} \,||\, R_B}{10}$ =0.00216mho

$C_i =\frac{1}{2\pi f X_{ci}}$ =1.47µF

Feedback factor, $\beta = -R_E = 1.2k\Omega$

$G_m = -h_{fe} / (h_{ie} + R_E) = -0.0263$

Desensitivity factor, $D = 1 + \beta\ G_m = -1.63$

Transconductance with feedback, $G_{mf} = G_m / D = 0.01613$

OBSERVATIONS:

V_S=20mv

S.NO	Frequency(Hz)	Output Voltage (V)	Gain=(V_0/V_i)	Gain in dB A_v=20 $\log_{10}$ (V_0/V_i)

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1) What is feedback?

2) What is positive feedback?

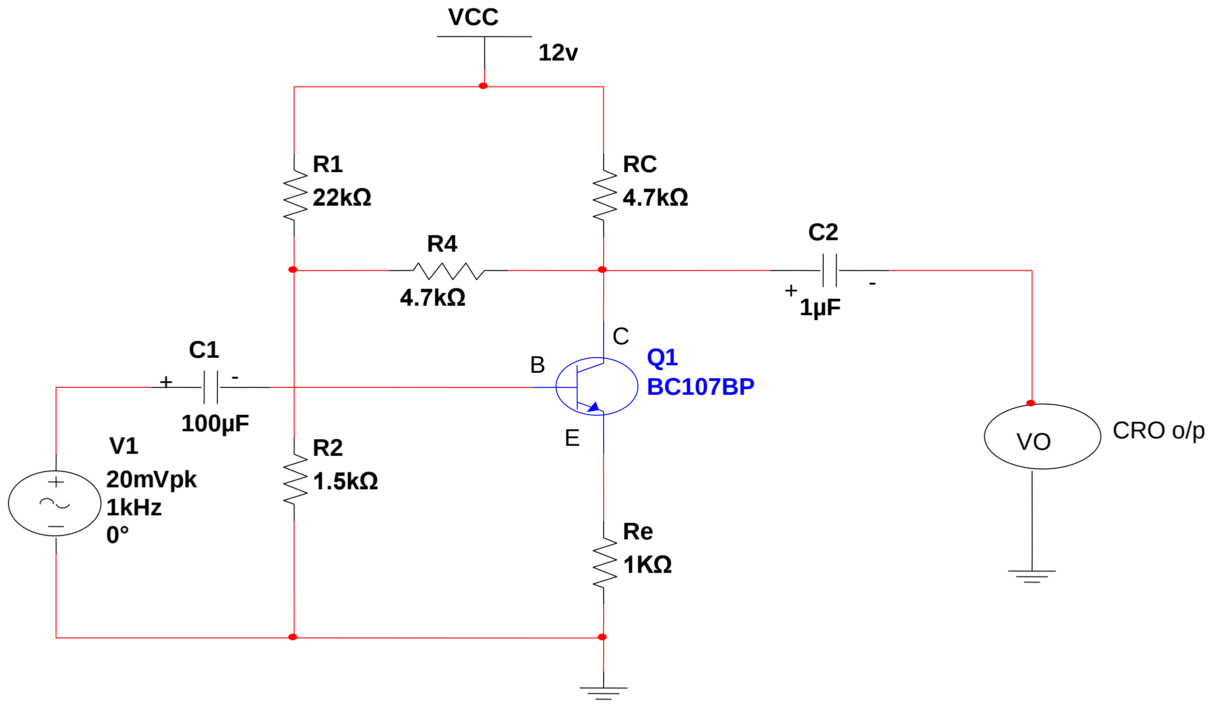
3) Define amplification factor?

4) What is Q-point?

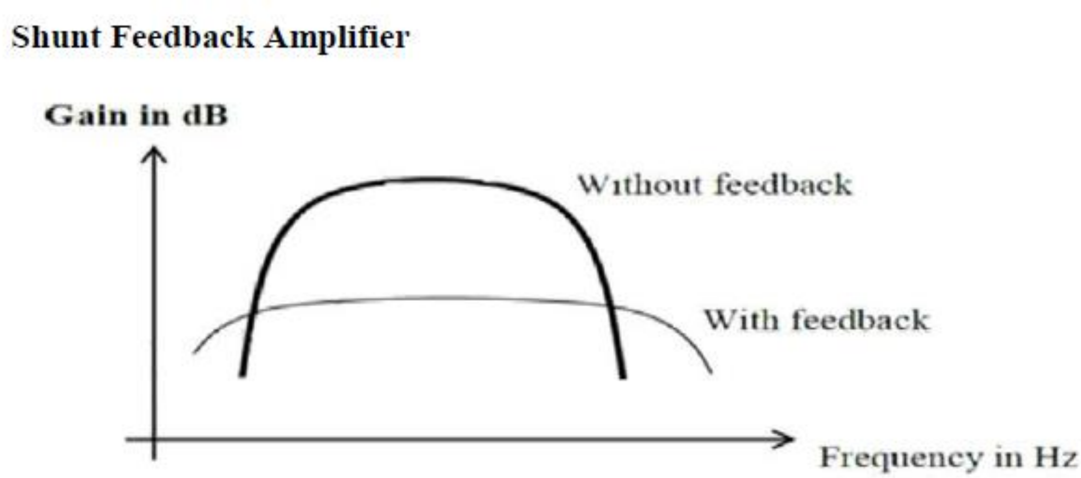
5) What is the effect of current series feedback amplifier on the input impedance of the amplifier?

CIRCUIT DIAGRAM:

Voltage shunt Feedback Amplifier



FREQUENCY RESPONSE



Exp No: 05 **Date:**

VOLTAGE SHUNT (SHUNT-SHUNT) FEEDBACK AMPLIFIER

AIM: To design and test the voltage shunt feedback amplifier and to calculate the following parameters with feedback.

1. Mid band gain.
2. Bandwidth and cut-off frequencies.

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	Transistor	BC107	1
2	Resistors	22kΩ	1
		1.5 kΩ	1
		4.7KΩ	2
		1KΩ	1
3	Capacitors	1µF, 100µF	1
4	RPS	0-30V	1
5	Function Generator	0-3MHz	1
6	CRO	30MHz	1
7	Bread board	-	1
8	Connecting wires	-	As Per Required

PROCEDURE:

1. Connect the circuit as per the circuit diagram.

2. Keeping the input voltage constant, vary the frequency from 50Hz to 3MHz in regular steps and note down the corresponding output voltage.

3. Plot the graph: Gain (dB) Vs Frequency

4. Calculate the bandwidth from the graph.

5. Calculate the input and output impedance.

6. Remove Emitter Capacitance, and follow the same procedures (1 to 5).

DESIGN PROCEDURE/ DESIGN CALCULATIONS:

V_{cc}=12V I_C= 1mA; A_V = 30; R_f =2.5KΩ ; s = 2;

$r_e = \frac{26mV}{I_C}$ =26Ω

$\beta = \frac{1}{R_f}$ =0.0004

h_{fe} =100

h_{ie} = h_{fe} r_e 2.6k **Ω**

$V_{ce} = \frac{V_{CC}}{2}$ =6 **V**

V_E = Vcc /10=1.2V

Applying KVL to output loop, we get;
$V_{cc} = I_E R_E + I_C R_C + V_{ce}$;
$12=1\times10^{-3}\times R_C+6+1.2$

R_C = 4.8 KΩ

Since I_B is very small when compare with I_C , $I_C \approx I_E$

$R_E = \frac{V_E}{I_E}$

=1.2k **Ω**
$S = 1+ \frac{R_B}{R_E}$
2=1+($R_{B/1.2K}$)

R_B =1.2KΩ
$V_B = \frac{V_{CC}R_2}{R_1+R_2}$

$0.7=\frac{12R2}{R1+R2}$

$\frac{R2}{R1+R2}$=0.05

$R_B = R_1 \,||\, R_2$

By substituting above equation we will get

R_1 =24KΩ,R2=1.5kΩ

Ro =Rc ‖ R_f R_i =(R_B || hie) R_f=0.1895

R_m = - (h_{fe}(R_B || R_f)(R_C|| R_f)) / ((R_B|| R_f) + h_{ie})

Desensitivity factor, D = 1+β R_m

=1.0000758

$R_{if} = \frac{Ri}{D}$ =2.19kΩ

R_{of} == $\frac{Ro}{D}$ =0.018Ω

$R_{mf} = \frac{Rm}{D}$

$X_{ci} = \frac{R_{if}}{10}$ =219mho

$C_i = \frac{1}{2\pi f Xct}$ =0.1μF

OBSERVATIONS: V_S=20mv

S.No	Frequency(hz)	Output Voltage (v_0)	Gain=(v_0/v_i)	Gain in db A_v=20 $\log_{10}$ (v_0/v_i)

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1) What is the difference between positive feedback and negative feedback?

2) What are the applications of feedback amplifiers?

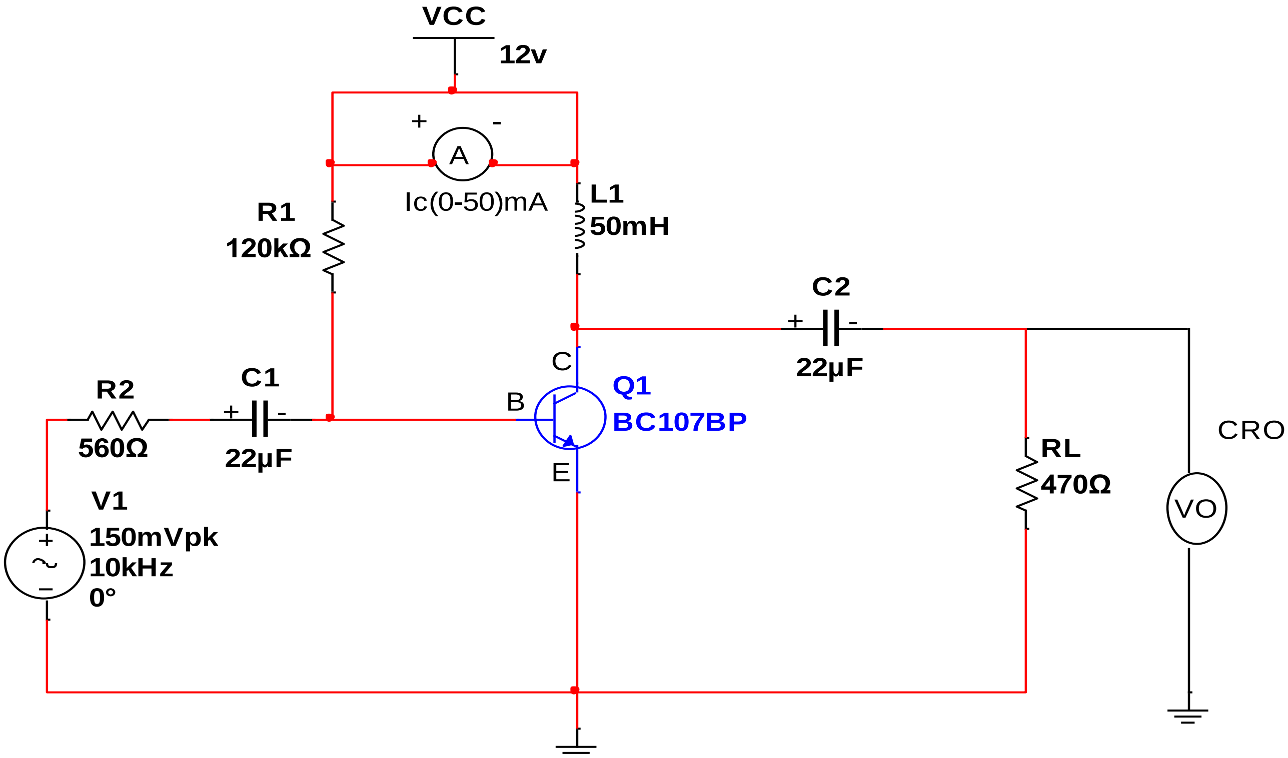
3) Mention the properties of negative feedback?

4) Give an example of negative shunt feedback?

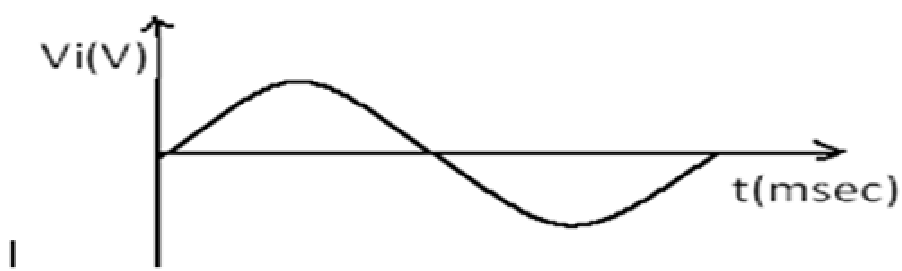
5) Define voltage shunt feedback?

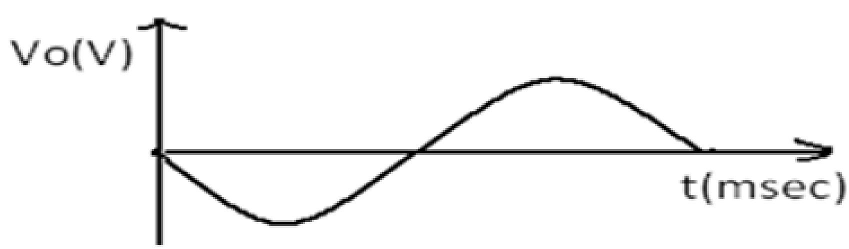
CIRCUIT DIAGRAM:

Class - A power amplifier



MODELWAVE FORMS:





Exp No: 06 **Date:**

CLASS – A POWER AMPLIFIER

AIM: To design a Class - A power amplifier using and compare practical efficiency with theoretical value.

APPARATUS:

S.NO	EQUIPMEN/COMPONENTS	RANGE	QUANTITY
1	TRANSISTOR	(SL100)	1
2	Resistors	120KΩ	1
		560Ω	1
		470Ω	1
3	Capacitors	22uF	2
4	DIB	50mH	1
5	Ammeter	0-50mA	1
6	RPS	0-30V	1
7	CRO	30MHz	1
8	Bread Board	-	1
9	Connecting Wires	-	As Per Required

OPERATION:

The above-shown circuit is a directly coupled Class A amplifier. An amplifier where the load is coupled to the output of the transistor using a transformer is called a direct coupled amplifier.
Using transformer coupling technique, the efficiency of an amplifier can be enhanced to a great extent. The coupling transformer provides good impedance matching between the load and output, and it is the main reason behind the improved efficiency.

Generally, the current flows through the collector resistive load, this will cause the wastage of the DC power in it. As a result, this DC power dissipated in the load in a form of heat, and it does not contribute any output AC power.

Hence it is not advisable to pass the current through the output device (ex: loudspeaker) directly. For this reason, a special arrangement done by using a suitable transformer for coupling the load to the amplifier as given in the above circuit.

The circuit has the potential divider resistors R1 & R2, biasing and emitter bypass resistor Re, used for circuit stabilization. The emitter bypass capacitor CE and emitter resistor Re are connected parallel to prevent AC voltage. The input capacitor Cin (Coupling Capacitor) used to couples AC input signal voltage to the base of the transistor and it blocks the DC from the previous stage.

DESIGN PROCEDURE/ DESIGN CALCULATIONS

Let V_{cc}=15V ,I_c=16mA , C=10µF

$R_L = \frac{Vcc}{2Ic} = 468\Omega \approx 470\Omega$

$R_B = \frac{Vcc-Vb}{Ibias} = \frac{15-0.7}{0.16} \approx 56\ K\Omega$

$I_B = \frac{Ic}{\beta} = \frac{16mA}{100} = 0.16mA$

PROCEDURE:

1. Connect the circuit as shown in figure.

2. Adjust input signal amplitude in the function generator and observe an amplified voltage at the output without distortion.

3. By keeping input signal voltage, say at 150 mV, vary the input signal frequency 10kHz as shown in tabular column and note the corresponding output voltage.

4. Measure and note down the zero signal dc current by disconnecting the function generator from the circuit.

5. Calculate the efficiency according to the expressions given.

6. Plot the graph between the o/p gain and frequency and calculate the bandwidth.

CALCULATIONS

$P_{dc}=(Vcc)^2/8R_L$

$P_{ac}=Vcc*Ic$

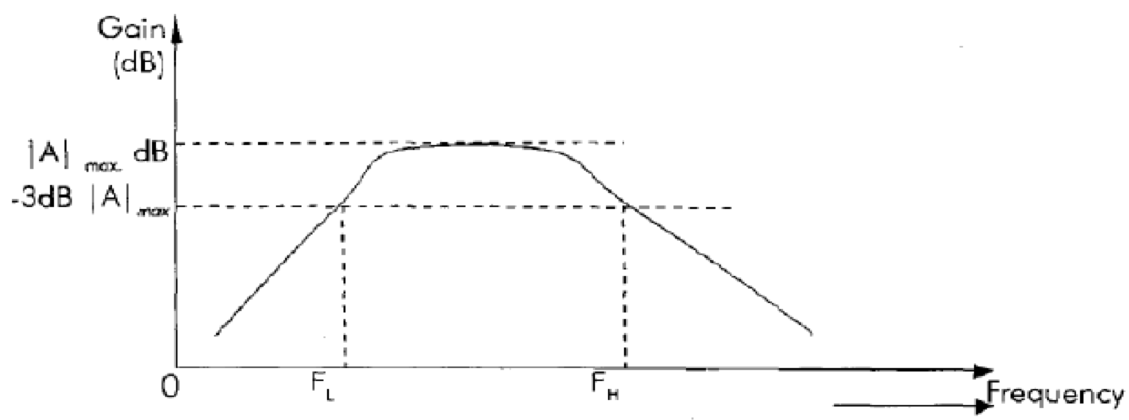
$\%\eta= P_{ac}/P_{dc}*100$

Efficiency $\%\eta$=

OBSERVATIONS: V_i =150mv

S.NO	FREQUENCY(Hz)	OUTPUT VOLTAGE (V_0)	GAIN (V_0/V_i)	GAIN IN dB A_v=20 $\log_{10}$ (V_0/V_i)

FREQUENCY RESPONSE



Bandwidth=$f_H - f_L$

PRECAUTIONS:

1. No loose contacts at the junctions.

2. Check the connections before giving the power supply

3. Observations should be taken carefully.

RESULT:

1. Frequency Response of CLASS-A Power amplifier is plotted.
2. Efficiency of CLASS A Power amplifier is found to be___________
3. Bandwidth $f_H - f_L$ = ____________
4. Efficiency (%η)=

CONCLUSION:

VIVA QUESTIONS:

1. What is the main difference between general amplifier and power amplifier?

2. Why can't we get more current and voltage gains using general amplifier?

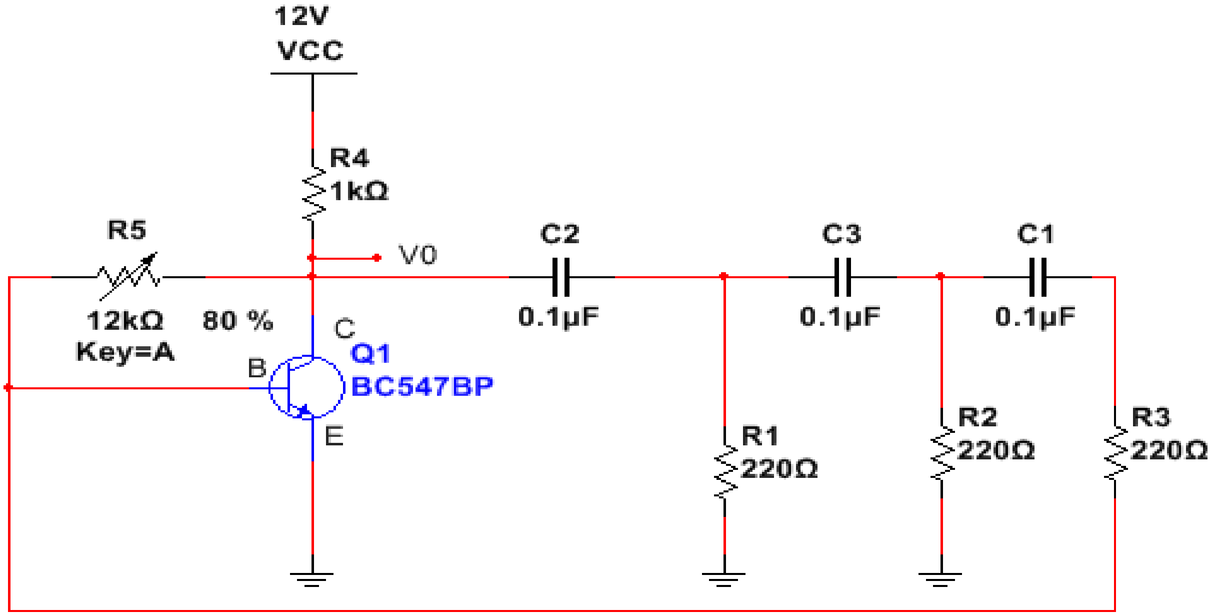
3. Is the power amplifier amplifies the power of input signal?

4. What are the classifications of Power amplifiers?

5. What does class A amplifier delivers?

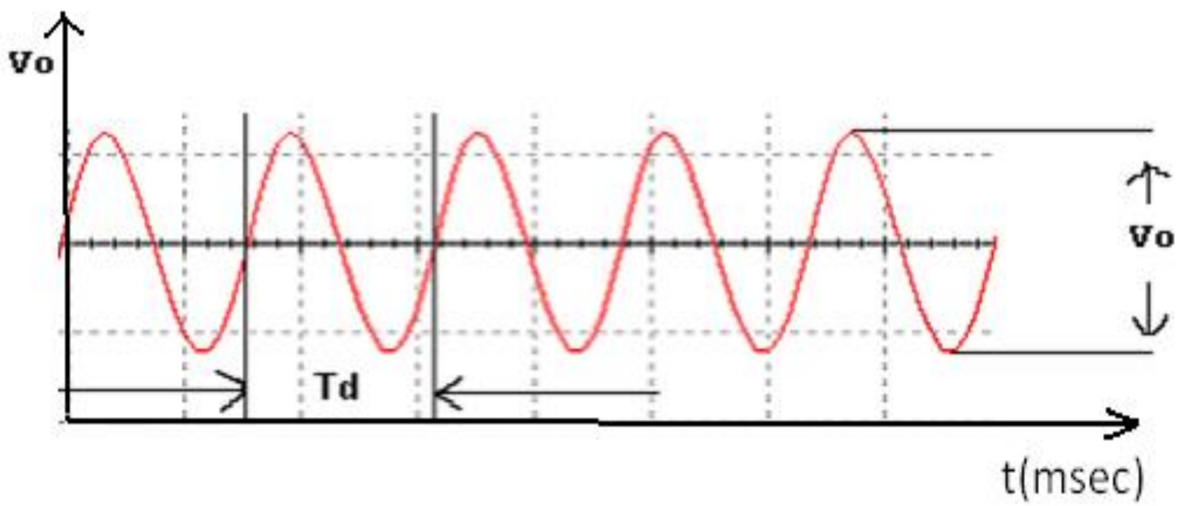
CIRCUIT DIAGRAM:

RC Phase Shift Oscillator:



MODELWAVE FORMS:

OUT PUT WAVEFORM:



OUTPUT WAVEFORM: $\theta = 60^0$

Exp No: 07 **Date:**

RC PHASE SHIFT OSCILLATOR

AIM: To design a RC phase shift oscillator and verify practical frequency with theoretical Frequency.

APPARATUS:

S.NO	EQUIPMEN/COMPONENTS	RANGE	QUANTITY
1	TRANSISTOR	BC547	1
2	Resistor	1kΩ	1
		220Ω	3
3	Capacitors	0.1µf	3
4	DRB	-	1
5	RPS	0-30V	1
6	CRO	30MHz	1
7	Bread Board	-	1
8	Connecting Wires	-	As Per Required

OPERATION:

When the circuit is switched on, current through R3 starts increasing because of biasing. This charging current induces voltage across R2 through C3.
The voltage across R2 leads the voltage across R3 by 60^0.since three R-C sections are provided, therefore, the phase shift circuit produces a total phase shift of $60x3=180^{0.}$
A further phase shift of $180^0$is produced due to the transistor properties. So a total shift of 360 degrees is produced.
Therefore a fraction of the output fed to the input is in phase with it.
The RC phase shift oscillator can be made variable by making the resistors or capacitors variable. The common approach is to leave the resistors untouched the three capacitors are replaced by a triple gang variable capacitor.

PROCEDURE:

1. Connections are made as per the circuit diagram.

2. Switch ON the power supply and set the biasing voltage V_{CC} =12V .

3. Adjust the 10KΩ pot to get a stable sinusoidal output and observe the sine wave form on oscilloscope.

4. Measure the frequency of oscillations of the output from the oscilloscope, then compare with theoretical value.

5. With respect to the output Vo, the waveforms at points TP_1, TP_2 and TP_3, are observed on oscilloscope. We can see the phase shift at each point being shifted by an angle 60_0, 120_0, 180_0.

6. Draw the waveform on graph sheet.

DESIGN:

Amplifier design

Let V_{cc}=12V, I_c=4mA, h_{fe}=100

Let V_E=2V, V_{ce}=6V

Therefore $R_E=V_E/I_E$

$= V_E/I_c$

$=2/4mA$

$=0.5K\Omega=500\Omega$

So use $R_E=470\Omega$

Apply KVL to the CE Loop

$V_{cc}-I_cR_c-V_{CE}-V_E=0$

$12-4R_c-6-2=0$

Therefore $R_c=1k\Omega$

Calculation of R_1 AND R_2

From biasing circuit

$V_B=V_{cc}\times \frac{R2}{R1+R2}$

We know that

$V_B=V_{BE}+VE=2+0.7$

$=2.7V$

Therefore $\frac{VB}{Vcc}=\frac{R2}{R1+R2}$

$\frac{2.7}{12}=\frac{R2}{R1+R2}$

$\frac{R2}{R1+R2}=0.225$

$0.225R_1+0.225R_2=R_2$

$R_1=3.44R_2$

If $R_2= 6.8k\Omega$, then $R_1=23.3k\Omega$

Use R_1=22kΩ

Use C_E=50μF or 47μF

Also C_c=0.1μF

Design of shifting network

The frequency of oscillations is determined by phase shifting network. The oscillating frequency for the above circuit is given by

$$f_0 = \frac{1}{2\pi RC\sqrt{6+4K}}$$

Where $k = \frac{R_c}{R}$ which is usually <I

Let $f_0 = 2KHz$ (Audio frequency range 20Hz to 20KHz) and R=2.2KΩ

Therefore $K = \frac{R_c}{R} = \frac{1K}{2.2K} = 0.454$

Therefore

$$f_0 = \frac{1}{2\pi RC\sqrt{6+4(0.454)}}$$

C=0.0121μF; use C=0.01μF

$$h_{fe(min)} = 23 + 29 \times \frac{R}{R_c} + 4 \times \frac{R_c}{R}$$

Where R_c=1KΩ and R=2.2KΩ (Phase shifting network)

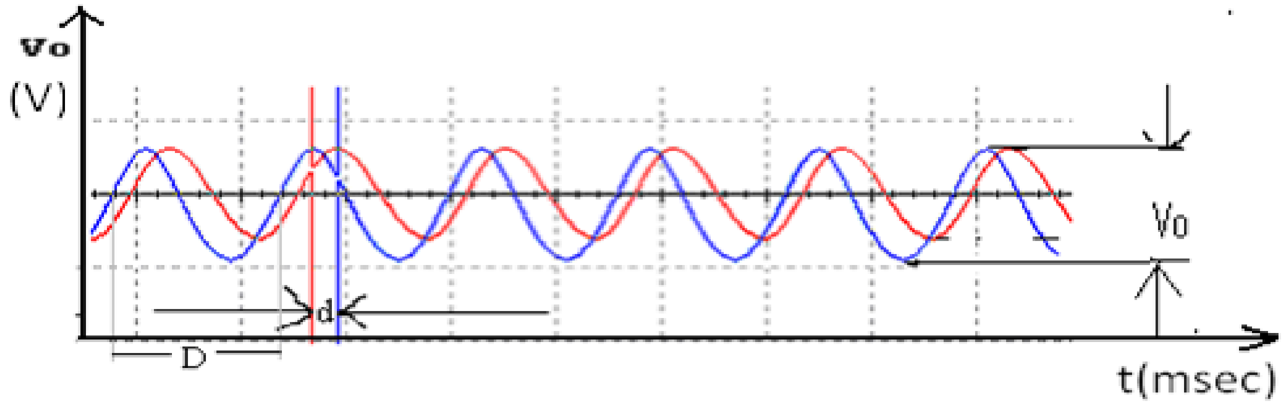
$$h_{fe(min)} = 23 + 29 \times \frac{2.2K}{1K} + 4 \times \frac{1K}{2.2K}$$

$$h_{fe(min)} = 89$$

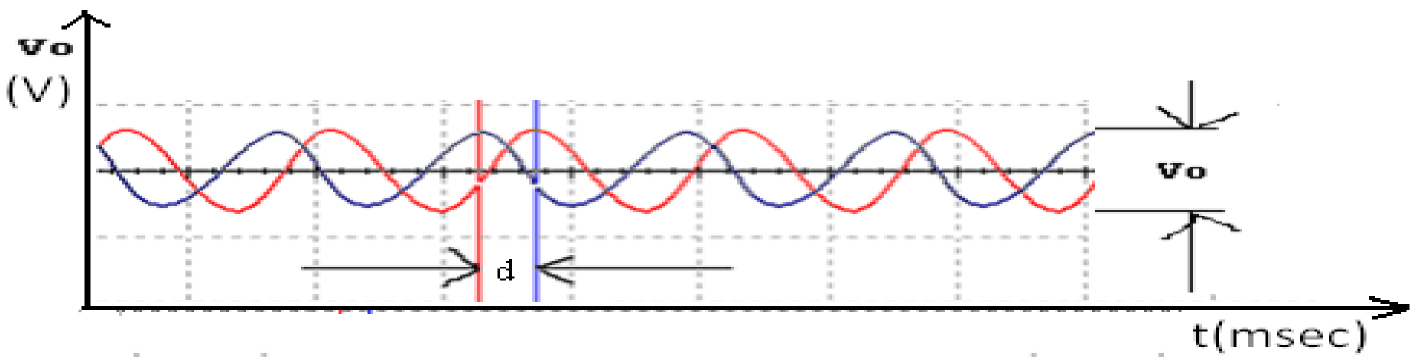
<u>THEORETICAL CALCULATIONS:</u>

C=0.1μF, R=220Ω

$$\boldsymbol{f_0 = \frac{1}{2\pi RC\sqrt{6}}}$$



OUTPUT WAVEFORM: θ = 120^0



OUTPUT WAVEFORM: θ = 180

OBSERVATIONS:

S.NO	RESISTANCE	CAPACITANCE	AMPLITUDE(V)	TIME PERIOD(ms)	TF	PF

RESULT:

Theoretical frequency of oscillations = _________KHz

Practical frequency of oscillations = _________KH

CONCLUSION:

VIVA QUESTIONS:

1. How does RC phase shift oscillator work?

2. What is RC phase shift?

3. What is the basic principle of oscillator?

4. What are the advantages of RC phase shift oscillator?

5. What is the gain of RC phase shift oscillator?

CIRCUIT DIAGRAM:

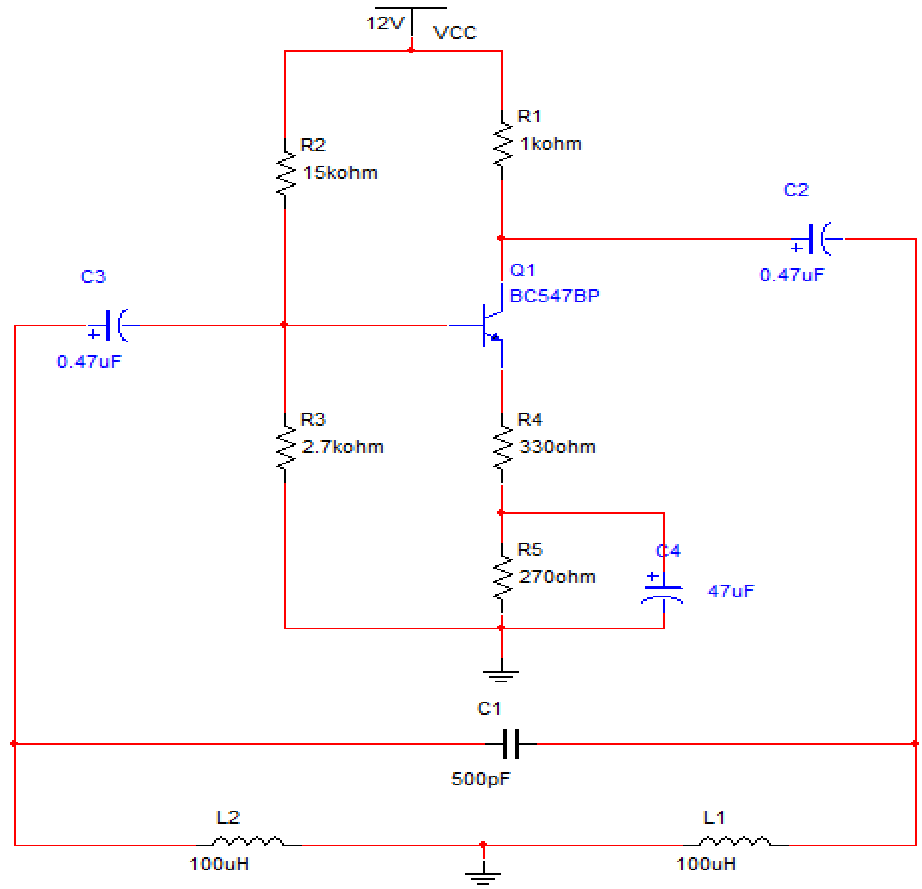
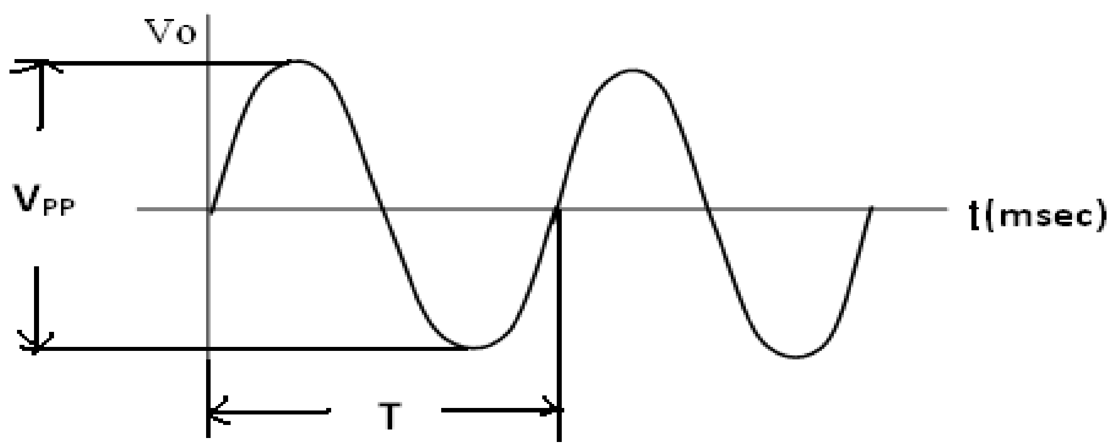


Fig: Hartley Oscillator

MODEL WAVE FORM:



Exp No: 08 **Date:**

HARTLEY OSCILLATOR

AIM: To determine the frequency of the Hartley oscillator and verify it to the theoretical value

APPARATUS:

S.NO	EQUIPMEN/COMPONENTS	RANGE	QUANTITY
1	TRANSISTOR	BC547	1
2	Resistors	15KΩ	1
		2.7KΩ	1
		1KΩ	1
		330 Ω	1
		270Ω	1
3	Capacitors	0.47µF	2
		500PF	1
4	DIB	100mH	2
5	DCB	500pf	1
6	RPS	0-30V	1
7	CRO	0-30MHz	1
8	Bread Board	-	1
9	Connecting Wires	-	As Per Required

OPERATION:

When the power supply is switched ON the transistor starts conducting and the collector current increases. As a result the capacitor C1 starts charging and when the capacitor C1 is fully charged it starts discharging through coil L1. This charging and discharging creates a series of damped oscillations in the tank circuit and it is the key. The oscillations produced in the tank circuit is coupled (fed back) to the base of Q1 and it appears in the amplified form across the collector and emitter of the transistor.

The output voltage of the transistor (voltage across collector and emitter) will be in phase with the voltage across inductor L1. Since the junction of two inductors is grounded, the voltage across L2 will be 180° out of phase to that of the voltage across L1. The voltage across L2 is actually fed back to the base of Q1. From this we can see that, the feed back voltage is 180° out of phase with the transistor and also the transistor itself will create another 180° phase difference. So the total phase difference between input and output is 360° and it is very important condition for creating sustained oscillations.

The frequency "F" of a Hartley oscillator can be expressed using the equation;

$$f = \frac{1}{2\pi\sqrt{LC}}$$

C is the capacitance of the capacitor C1 in the tank circuit.

L = L1+L2, the effective series inductance of the inductors L1 and L2 in the tank circuit.

Here the coils L1 and L2 are assumed to be winded on different cores. If they are winded on a single core then L=L1+L2+2M where M is the mutual inductance between the two coils.

DESIGN PROCEDURE/ DESIGN CALCULATIONS:

Transistor: **BC 107**

Let V_{CC} = 12V; I_C = 4.5 mA; V_E = 1.2V; V_{CE} =6V;

h_{FE} =100.

Given V_E = 1.2V. Therefore $R_E = V_E / I_E \approx V_E / I_C$ =266.67Ω; **R_E=270Ω**

Writing KVL for the Collector loop we get, $V_{CC} = I_C R_C + V_{CE} + V_E$

$R_C = (V_{CC} – V_{CE} – V_E) / I_C$ = (12-6-1.2)V/4mA=1.06KΩ; **R_C= 1 K Ω**

$h_{FE} R_E = 10R_2$

Assume **R_2=2.7KΩ,**

$V_B = (V_{cc} \times R_2) / (R_1 + R_2)$

Hence R1 = 14.14 K Ω ; **R1 = 15 K Ω**

□

Use **C_{C1}= 0.47µF**

Use **C_{C2}= 0.47 µF**

Use **C_E=47µF**

Hartley Oscillator

Oscillator Frequency $f=c.L_{eq.} =c. (L_1+ L_2)$

Assume f = 500 KHz. With $L_1 = L_2$ =100µH,

we get

$L_{eq.} = L_1+ L_2$ = 200µH

$L_{eq.}C=1/(2\pi f)^2=(\pi)^{-2}x10^{-12}$

This gives C = {1/ $(\pi)^2$ x 200µH} pF =500pF

Use C = 470 pF

For this capacitance value ***f*= 518.6 KHz**

THEORETICAL CALCULATIONS:

C = 500pF, LT = 100mH+100mH (L_1+L_2)

$$f = \frac{1}{2\pi\sqrt{LC}}$$

PROCEDURE:

1. Connect the circuit diagram as shown in the figure
2. Set V_{CC} = 12V
3. Keep the capacitance of the decade capacitance box, and measure the generated output signal amplitude and frequency from CRO.
4. Vary the Inductance in steps and note down frequency and amplitude at each.
5. Plot the graph from CRO and verify the practical frequency with theoretical frequency.

TABULAR COLUMN:

C (µf)	L_1 (mH)	L_2 (mH)	Theoretical F(hz)	Practical Time period	Practical F(hz)	Amplitude (v)

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What is the use of Hartley oscillator?

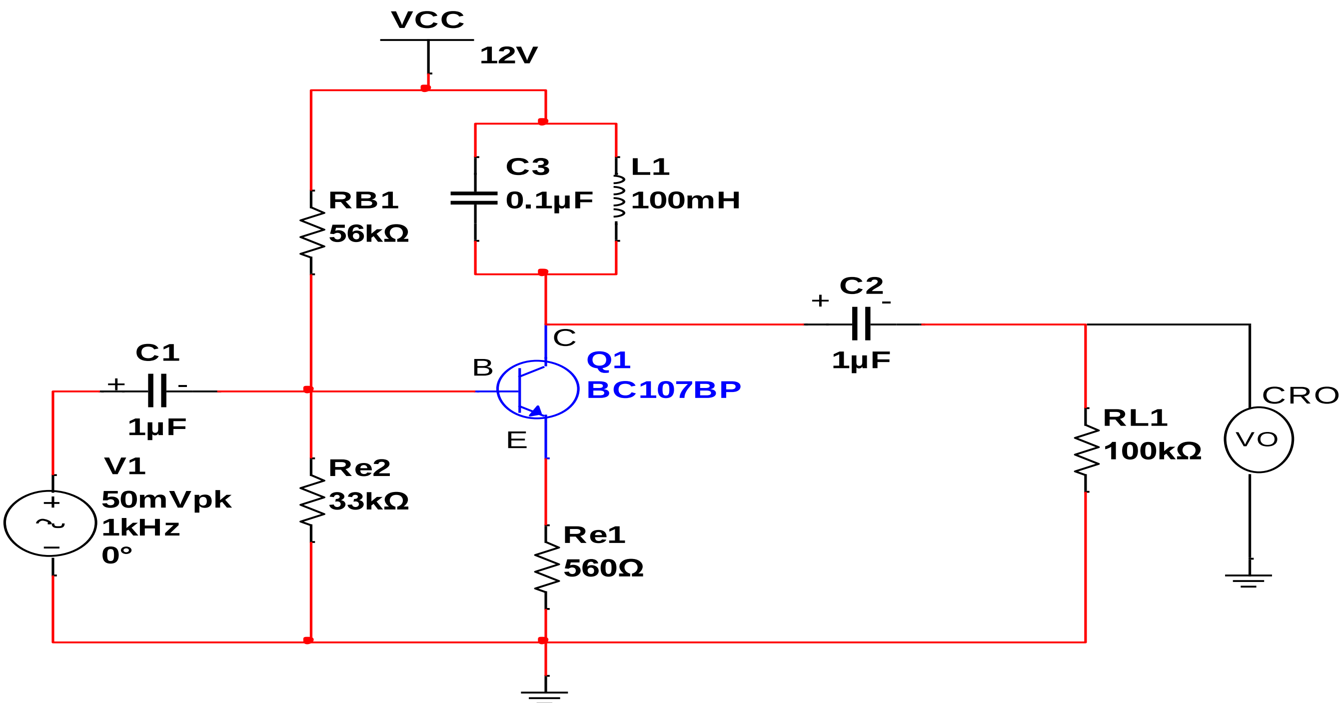
2. What are the advantages of Hartley oscillator?

3. Recommended frequency range of Harley oscillator is?

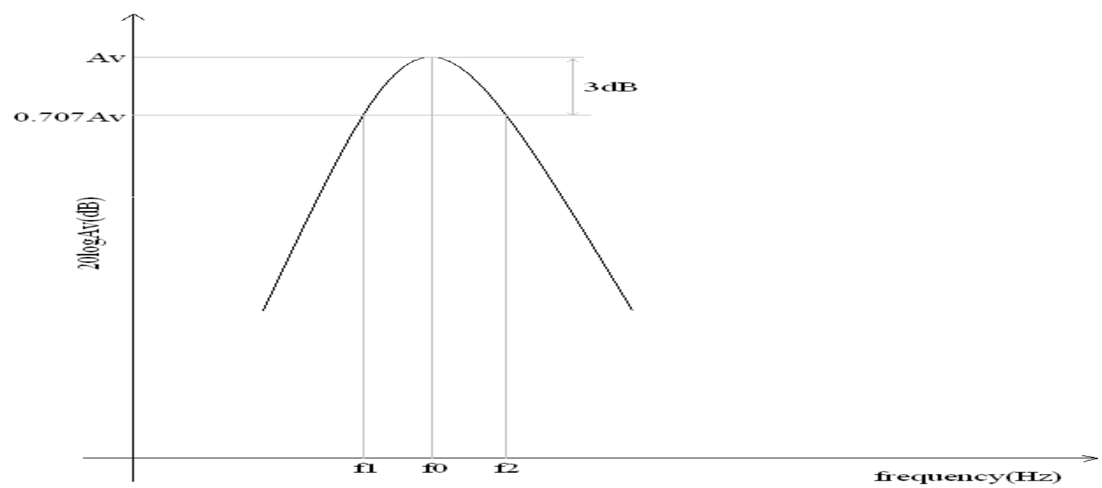
4. Which component of Hartley oscillator is used in the feedback system?

5. Which network is used to give feedback to transistor of Hartley oscillator?

CIRCUIT DIAGRAM: SINGLE TUNED VOLTAGE AMPLIFIER



MODEL GRAPH:



Exp No: 09 **Date:**

SINGLE TUNED VOLTAGE AMPLIFIER

AIM: To design single tuned voltage amplifier and verify practical frequency with theoretical frequency.

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	Transistor	BC 107BP	1
2	Resistors	100KΩ	1
		56KΩ	1
		33KΩ	1
		560Ω	1
3	Capacitors	1μF	2
		0.1μF	1
4	DIB	100mH	1
5	Function generator	0-30MHz	1
6	RPS	0-30V	1
7	CRO	30MHz	1
8	Bread board	-	1
9	Connecting wires	-	As Per Required

OPERATION:

The circuit operation of single tuned amplifiers begins with the application of the high-frequency signal that is to be amplified at the base-emitter terminal of the transistor, shown in the figure above. By varying the capacitor employed in the tuned circuit, the resonant frequency of the circuit can be made equivalent to the frequency of the applied input signal. Here, the high impedance is offered to the signal frequency by the tuned circuit. Thus, a large output is achieved. For an input signal with multiple frequencies, only the frequency that corresponds to resonant frequency will get amplified. While all other frequencies are rejected the LC circuit. Hence, only the desired frequency signal gets selected and thus amplified by the circuit.

CALCULATIONS:

L =100mH, C = 0.1μF

Theoretical frequency f = $1/2\pi\sqrt{C\,L}$

PROCEDURE:

1. Connections are made as per the circuit diagram.
2. A signal of 1 KHz frequency and 50mV peak-to-peak of sine wave is applied at the Input of amplifier.
3. By keeping the input voltage constant, vary the frequency from 1 KHz to 2 KHz in regular steps and note down the corresponding output voltage.
4. Calculate practically the frequency of oscillations by using the expression.

$f = 1/T_d$ (T_d= Time period) and compare it with the theoretical frequency $f = 1/2\pi\sqrt{C L}$

5. Voltage gain in dB is calculated by using the expression $A_v=20\log_{10}(V0/V_i)$
6. Plot graph for gain (A_v) in dB vs frequency in Hz on a semi log graph.
7. The Bandwidth of the amplifier is calculated from the graph using the Expression,

Bandwidth $BW=f_2-f_1$

Where f_1 is lower 3 dB frequency, f2 is upper 3 dB frequency

OBSERVATIONS:

` V_i=20mV

S.NO	FREQUENCY(Hz)	OUTPUT VOLTAGE (V)	GAIN (V_0/V_i)	GAIN IN dB $A_v=20\log_{10}(V_0/V_i)$

RESULT:

Bandwidth $BW=f_2-f_1$

theoretical frequency $f = 1/2\pi\sqrt{C L}$

CONCLUSION:

VIVA QUESTIONS:

1. What is tuned amplifier? What are the various types of tuned amplifiers?

2. Define tuned amplifier?

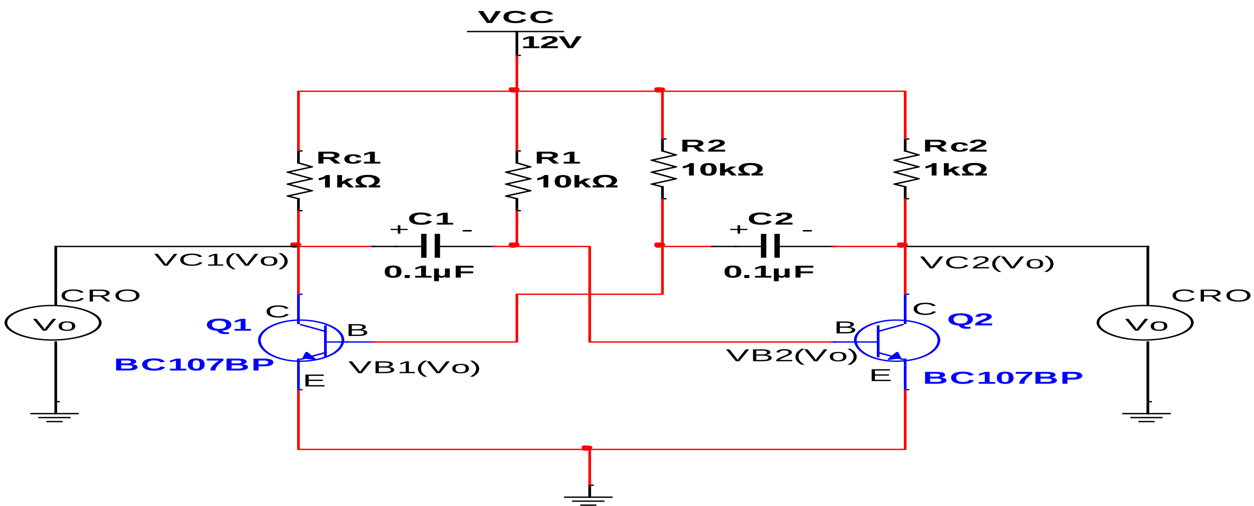
3. Why tuned amplifier cannot be used at low frequency?

4. What is the other name for tuned amplifier?

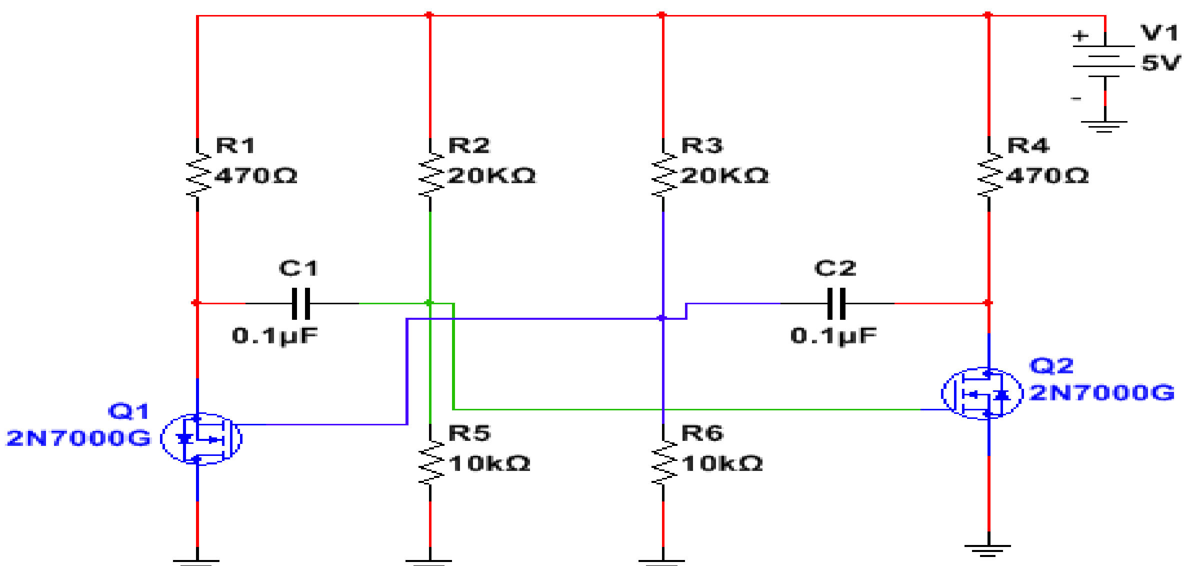
5. Mention the Two Applications of tuned amplifiers?

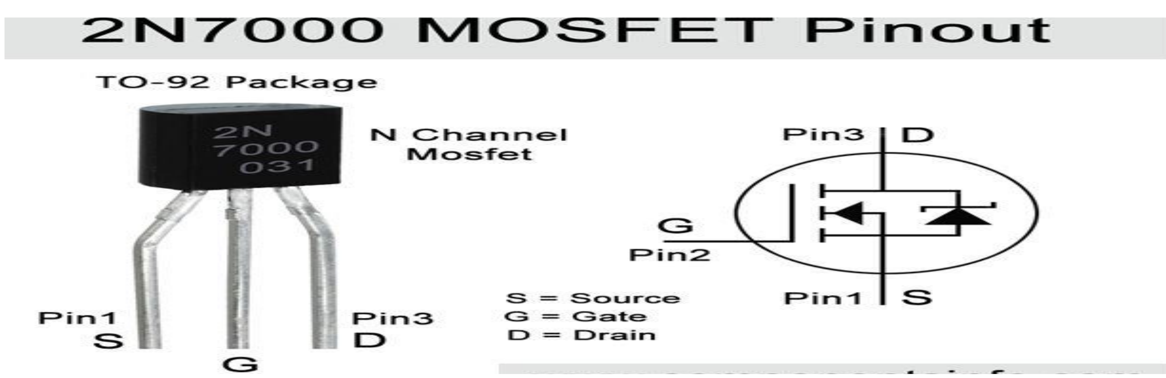
CIRCUIT DIAGRAM:

ASTABLE MULTIVIBRATOR Using (BJT):



ASTABLE MULTIVIBRATOR Using MOSFET:





Exp No: 10 **Date:**

ASTABLE MULTIVIBRATOR

AIM: To Design an Astable Multivibrator to generate a square wave of 1 KHz frequency using Transistor.

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	BJT & MOSFET	BC107 (or)2N7000	2
2	Resistors	1KΩ, 10KΩ (BJT)	2
		20k Ω,10k Ω,470 Ω (MOSFET)	1
3	Capacitors	1µF	2
		0.1µF	2
4	Function generator	0-30MHz	1
5	RPS	0-30V	1
6	CRO	30MHz	1
7	Bread board	-	1
8	Connecting wires		As Per Required

OPERATION:

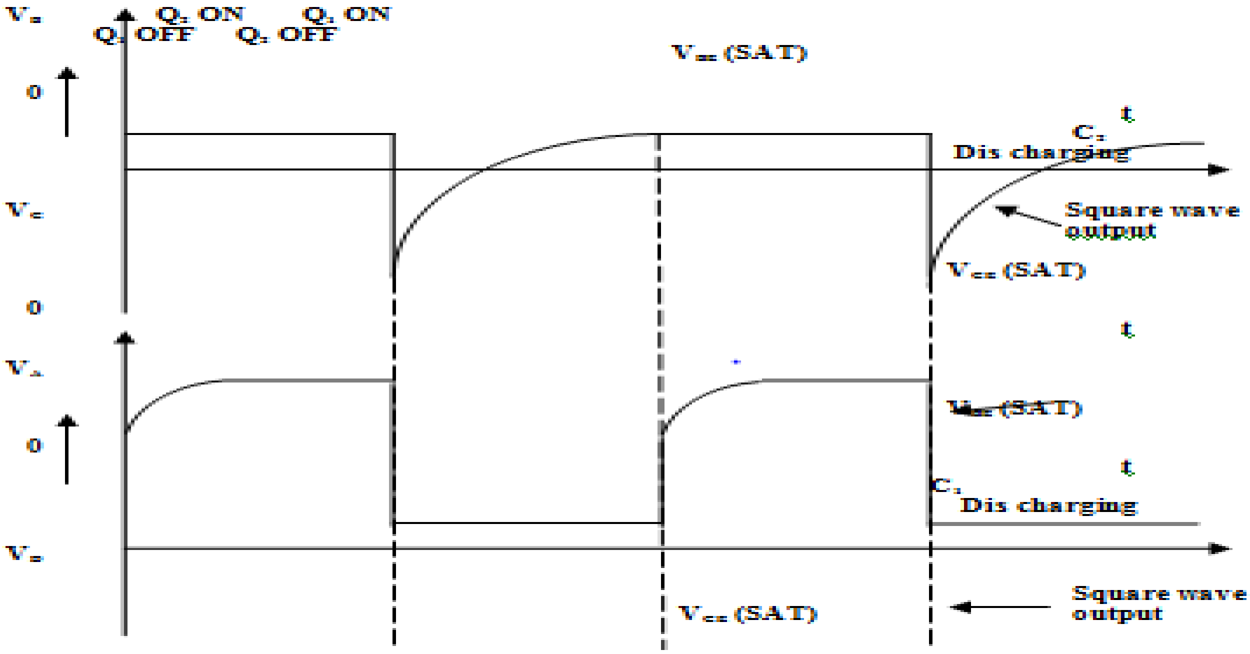
When the power is applied, due to some imbalance in the circuit, the transistor Q_2 conducts more than Q_1 i.e. current flowing through transistor Q_2 is more than the current flowing in transistor Q_1. The voltage V_{C2} drops. This drop is coupled by the capacitor C_1 to the base by Q_1 there by reducing its forward base-emitter voltage and causing Q_1 to conduct less. As the current through Q_1 decreases, V_{C1} rises. This rise is coupled by the capacitor C_2 to the base of Q_2. There by increasing its base- emitter forward bias. This Q_2 conducts more and more and Q_1 conducts less and less, each action reinforcing the other. Ultimately Q_2 gets saturated and becomes fully ON and Q_1 becomes OFF. During this time C_1 has been charging towards V_{CC} exponentially with a time constant $T_1 = R_1C_1$. The polarity of C_1 should be such that it should supply voltage to the base of Q_1. When C_1 gains sufficient voltage, it drives Q_1 ON. Then VC1 decreases and makes Q_2 OFF. V_{C2} increases and makes Q_1 fully saturated. During this time C_2 has been charging through V_{CC}, R_2, C_2 and Q_2 with a time constant $T2 = R_2C_2$. The polarity of C_2 should be such that it should supply voltage to the base of Q_2. When C_2 gains sufficient voltage, it drives Q_2 On, and the process repeats.

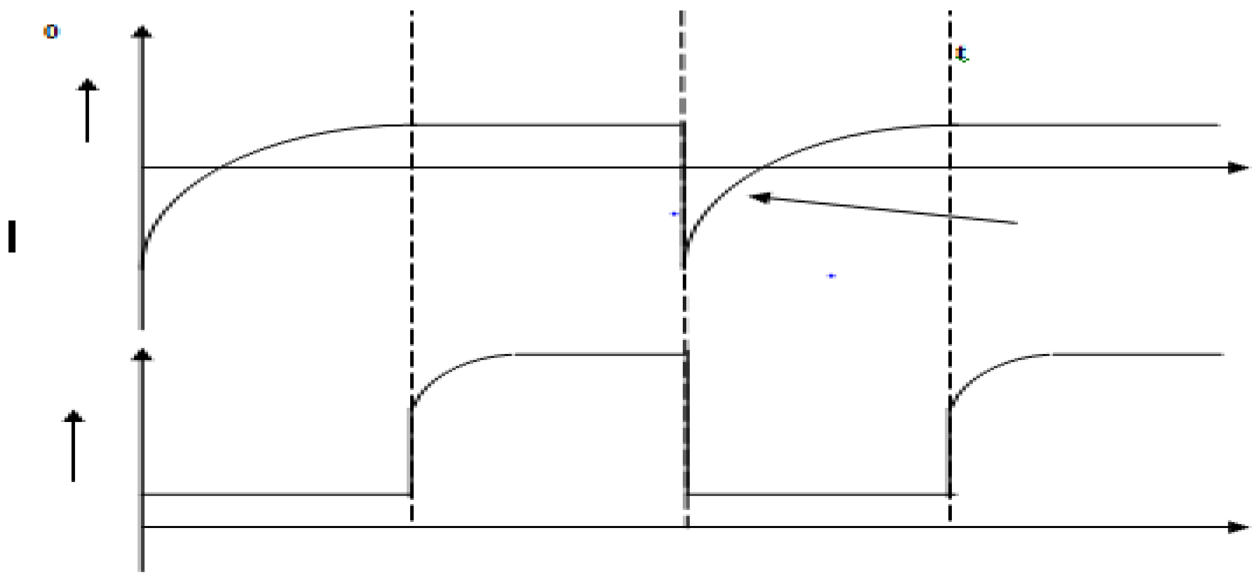
THEORETICAL CALCULATIONS:

$F = 1/ T = (1/1.38RC)$

$R = 10K\Omega \quad C = 0.1\mu F$

MODEL GRAPH:





TABULAR COLUMN:

Practical values	Amplitude (v)	Practical Time period	Practical F(hz)
V_{C1} = Voltage at collector of Q_1			
V_{B2} = Voltage at base of Q_2			
V_{C2} = Voltage at collector of Q_2			
V_{B1} = Voltage at base of Q_1			

<u>Design Procedure:</u>

The period T is given by

$T = T_1 + T_2 = 0.69\ (R_1C_1 + R_2C_2)$

For symmetrical circuit, with $R_1 = R_2 = R$ & $C_1 = C_2 = C$

$T = 1.38\ RC$

Let $V_{CC} = 12V$; $h_{fe} = 51$ (for BC107), $V_{BESat} = 0.7V$; $V_{CESat} = 0.3V$ Let $C = 0.1\mu F$ & $T = 1mSec$.

$10^{-3} = 1.38 \times R \times 0.1 \times 10^{-6}$

$R = 7.24K\Omega$ (Practically choose $10K\Omega$) i.e., R1 and R2 resistors.

Let I_{Cmax}=10mA

$R_C = \frac{V_{cc} - V_{cesat}}{I_{cmax}} = \quad = \frac{12-0.3}{0.01}$

$R_C = \ = 1.17K\Omega$ ($1K\Omega$ is selected for Rc1 and Rc2)

PROCEDURE:

1. Make then connections as per the circuit diagram.
2. Observe the Base Voltage and Collector Voltages of Q1 & Q2 on CRO in DC mode and measure the frequency (f = 1/T).
3. Trace the waveforms at collector and base as each transistor with the help of dual trace CRO and plot the waveforms.
4. Verify the practical output frequency with theoretical values f = 1/T, where T = 1.38 RC

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What are the other names of Astable multivibrator?

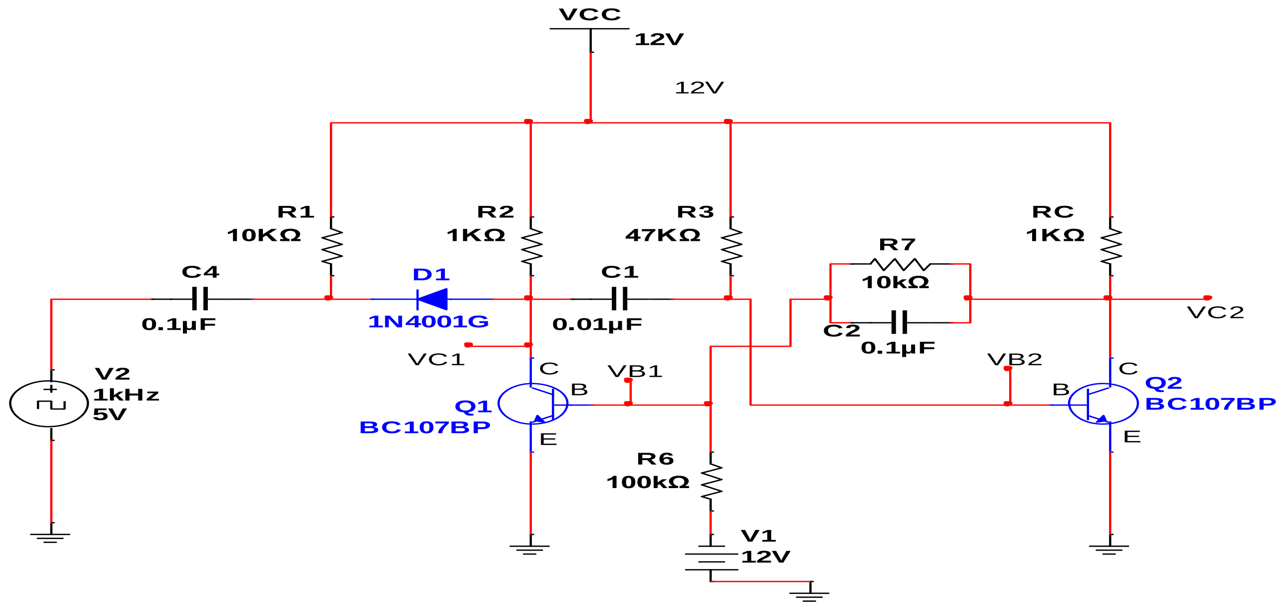
2. Define quasi stable state?

3. Is it possible to change time period of the waveform without changing R & C?

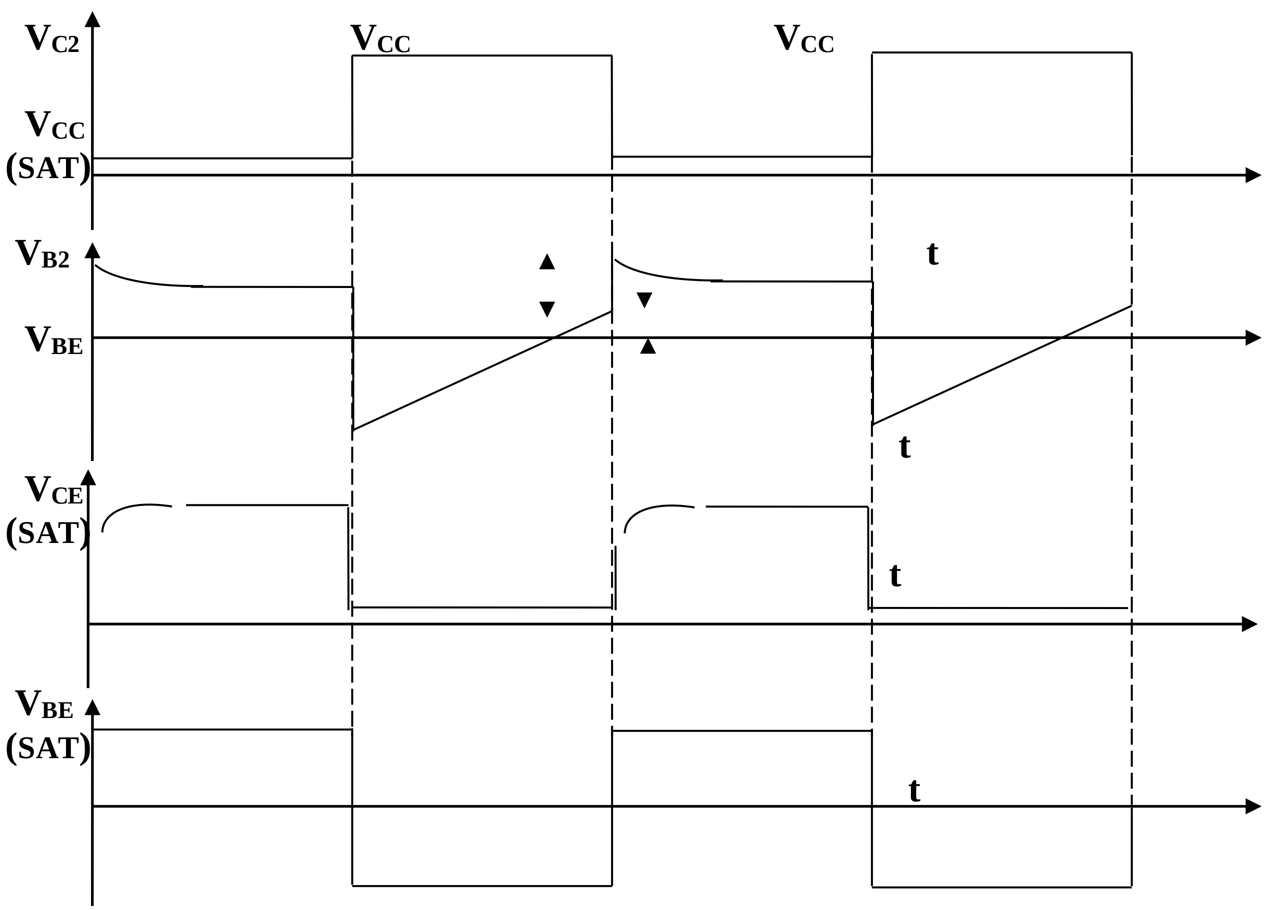
4. Explain charging and discharging of capacitors in an Astable Multivibrator?

5. How can an Astable multivibrator be used as VCO?

CIRCUIT DIAGRAM: MONOSTABLE MULTIVIBRATOR



MODEL WAVEFORMS:



Exp No:11 **Date:**

MONOSTABLE MULTIVIBRATOR

AIM: To Design a Monostable Multivibrator for the pulse width of 0.3msec

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	TRANSISTOR	BC107	2
2	Resistors	100KΩ	1
		47KΩ	1
		10KΩ	2
		1KΩ	2
3	Capacitors	0.1μF	2
		0.01μF	1
4	Diode	IN 4007	1
5	Function generator	0-30MHz	1
6	RPS	0-30V	1
7	CRO	30MHz	1
8	Bread board	-	1
9	Connecting wires	-	As Per Required

OPERATION:

Assume initially transistor Q_2 is in saturation as it gets base bias from V_{CC} through R. coupling from Q_2 collector to Q_1 base ensures that Q1 is in cutoff. If an appropriate negative trigger pulse applied at collector of Q_1 (V_{C1}) induces a transition in Q_2, then Q2 goes to cutoff. The output at Q_2 goes high. This high output when coupled to Q_1 base, turns it ON. The Q_1 collector voltage falls by I_{C1} R_{C1} and Q2 base voltage falls by the same amount, as voltage across a capacitor 'C' cannot change instantaneously.

The moment, a negative trigger is applied at V_{C1}, Q_2 goes to cutoff and Q_1 starts conducting. There is a path for capacitor C to charge from V_{CC} through R and the conducting transistor Q_1. The polarity should be such that Q_2 base potential rises. The moment, it exceeds Q_2 base cut-in voltage, it turns ON Q_2 which due to coupling through R1 from collector of Q2 to base of Q1, turns Q1 OFF. Now we are back to the original state i.e. Q_2 is ON and Q1 is OFF. Whenever trigger the circuit into the other state, it cannot stay there permanently and it returns back after a time period decided by R and C. Pulse width is given as T = 0.69RCsec.F

TABULAR COLUMN:

Practical values	Amplitude (v)	Practical Time period	Practical F(hz)
V_{C1} = Voltage at collector of Q_1			
V_{B2} = Voltage at base of Q_2			
V_{C2} = Voltage at collector of Q_2			
V_{B1} = Voltage at base of Q_1			

THEORETICAL CALCULATIONS:

T_{ON} = 0.69 RC   R= 47K%u2126 and C = 10nF or 0.01µF

Design Procedure:

To design a monostable multivibrator for the Pulse width of 0.3 mSec.

Let I_{Cmax} = 15mA, V_{CC} = 15V, V_{BB} = 15V, R_1 = 10K%u2126.   T =0.69RC

Choose C = 10nf (0.01µF)   T = 0.69 RC

$$0.3 \times 10^{-3} Sec = 0.69 \times R \times 10 \times 10^{-9}$$

$$R = 43.47 \text{ Kohms} \approx 47 \text{Kohms}$$

$$R_C = (V_{CC} - V_{CESAT}) / I_{CMAX} = (15 - 0.3) / 15 \times 10^{-3} = 1 \text{ K ohms}$$

Minimum requirement of $|V_{B1}| \leq 0.1$

For more margin, given V_{B1} = -1.185

$$V_{B1} = \frac{-V_{BB}}{R1+R2} R1 + \frac{-V_{CEsat}}{R1+R2} R2$$

Substitute the values, R_1=10kohms   we will get R2= 100Kohms

PROCEDURE:

1. Make the connections as per the circuit diagram.
2. Select the triggering pulse such that the frequency is less than 1/T
3. Apply the triggering input to the circuit and to the CRO's channel and Connect the CRO channel-2 to the collector and base of the Transistor Q1&Q2.
4. Adjust the triggering pulse frequency to get stable pulse on the CRO and now measure the pulse width and verify with the theoretical value.
5. Obtain waveforms at different points like V_{B1}, V_{B2}, V_{C1} & V_{C2} and plot the graph.

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What is a multivibrator?

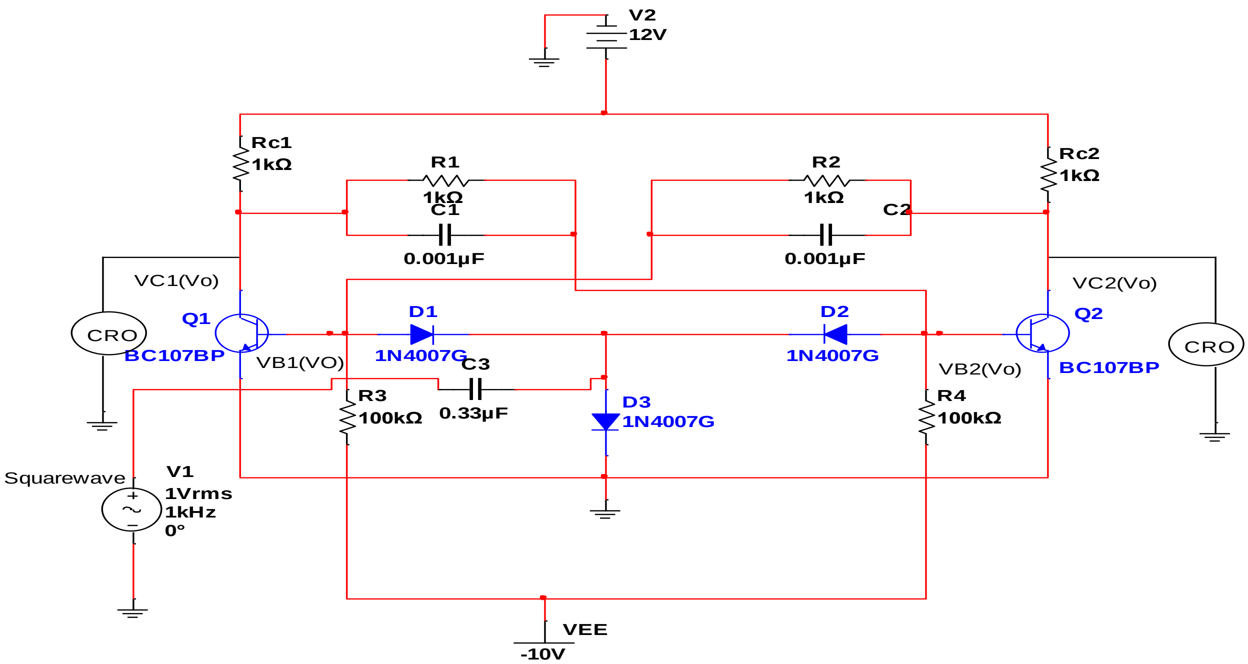
2. What are applications of Monostable Multivibrator?

3. The monostable multivibrator is also called as ----------.

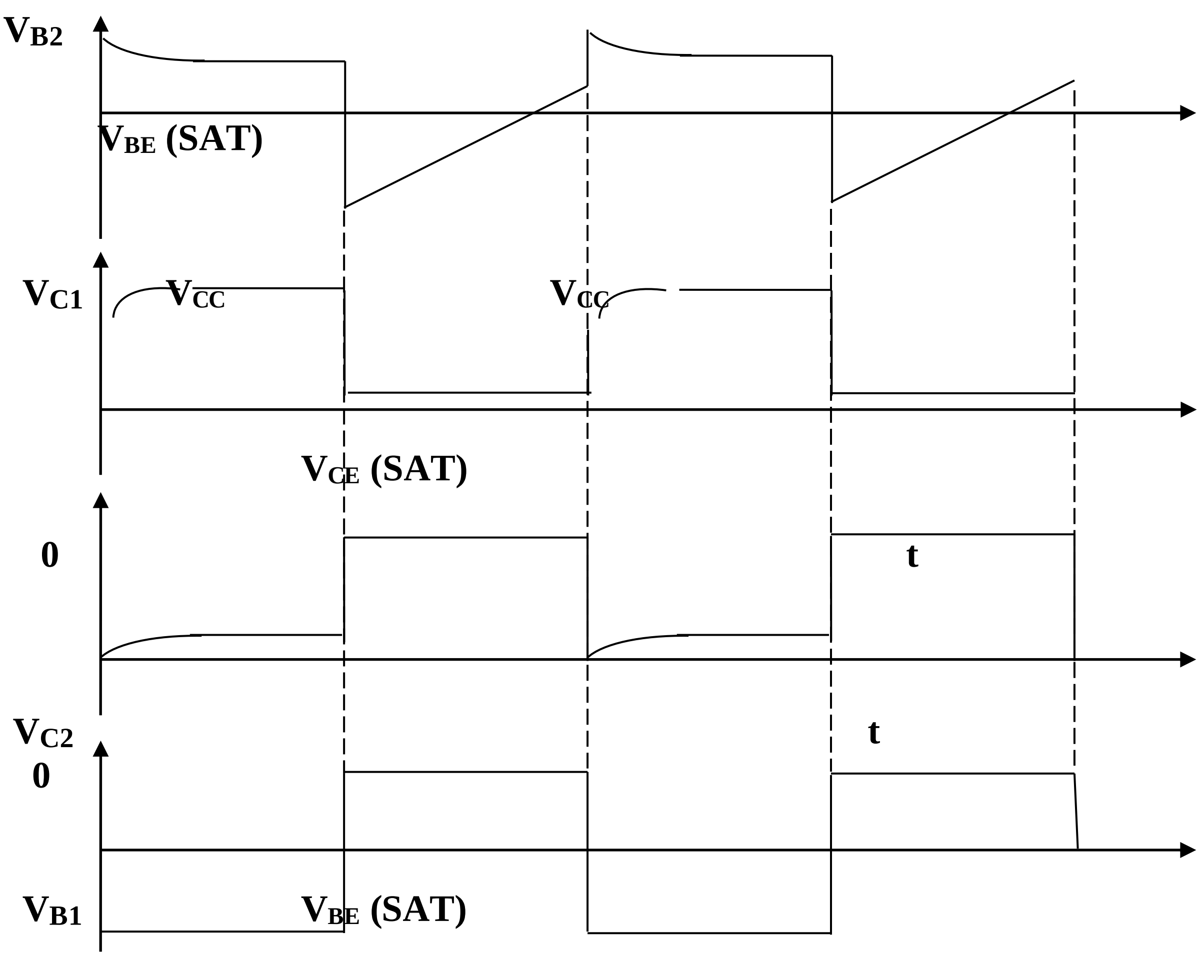
4. A Monostable Multivibrator generates wave

5. Why is the time period T also called Delay time?

CIRCUIT DIAGRAM: Bistable MultiVibrator:



MODEL WAVEFORM:



Exp No:12 **Date:**

BITABLE MULTIVIBRATOR

AIM: To Design Bistable Multivibrator to generate a square wave of 55 KHz frequency using Transistor.

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	TRANSISTOR	(BC 107)	2
2	Resistors	1KΩ	4
		100 KΩ	2
3	Capacitors	0.001µF,0.33 µF	2
4	Diode	IN4007	4
5	Function generator	0-30MHz	1
6	RPS	0-30V	1
7	CRO	30MHz	1
8	Bread board	-	1
9	Connecting wires	-	As Per Required

OPERATION:

When VCC is applied, one transistor will start conducting slightly more than that of the other, because of some differences in the characteristics of a transistor. Let Q_2 be ON and Q_1 be OFF. When Q_2 is ON, The potential at the collector of Q_2 decreases, which in turn will decrease the potential at the base of Q_1 due to potential divider action of R_1 and R_2. The potential at the collector of Q_1 increases which in turn further increases the base to emitter voltage at the base of Q_2. The voltage at the collector of Q_2 further decreases, which in turn further reduces the voltage at the base of Q_1. This action will continue till Q_2 becomes fully saturated and Q_1 becomes fully cutoff.

Thus the stable state of binary is such that one device remains in cut-off and other device remains at saturation. It will be in that state until the triggering pulse is applied to it. It has two stable states. For every transition of states triggering is required. At a time only one device will be conducting

THEORETICAL CALCULATIONS:

PROCEDURE:

1. Make the connections as per the circuit diagram.
2. Apply trigger pulse of 1 KHz 5v (p-p) from function generator.
3. Obtain waveforms at different points such as V_{B1}, V_{B2}, V_{C1} & V_{C2}.
4. Trace the waveform at collector and base of each transistor with the help of dual trace CRO. Note the Time relation of waveform

Design Procedure:

$$R_C=\frac{(V_{CC}-V_{CEsat})}{I_{Cmax}}$$

$$=\frac{15-0.3}{15*10^{-3}}=1k\Omega$$

$$V_{B1}=\frac{-V_{BB}}{R1+R2}R1+\frac{-V_{CEsat}}{R1+R2}R2$$

$-1.2 = (-15R_1 + 0.2R_2) /(R_1 + R_2)$; given R1=10KΩ

R2 = 100KΩ

R_1 = 10KΩ, R_2 = 100KΩ and C = 0.1μF

$F_{max} = (R_1 + R_2)/2C\, R_1 R_2$

$= (10 + 100) X 10^3 / (2 X 0.3 X 10^{-6} X 10 X 100 X 10^6) = 55$ KH

TABULAR COLUMN:

Practical values	Amplitude (v)	Practical Time period	Practical F(hz)
V_{C1} = Voltage at collector of Q_1			
V_{B2} = Voltage at base of Q_2			
V_{C2} = Voltage at collector of Q_2			
V_{B1} = Voltage at base of Q_1			

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What are the other names of Bistable Multivibrator?

2. What are the applications of a Bistable Multivibrator?

3. Describe the operation of commutating capacitors?

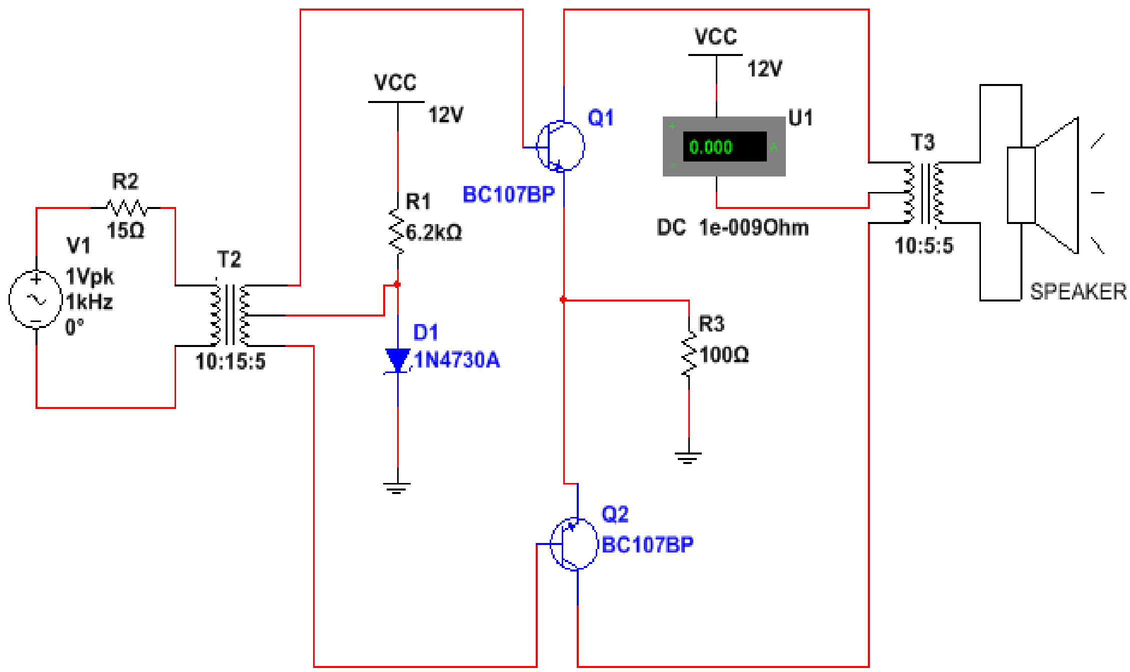
4. Commutating capacitors are also called as __ or __ .

5. What is the meaning of a stable state in a multi-vibrator?

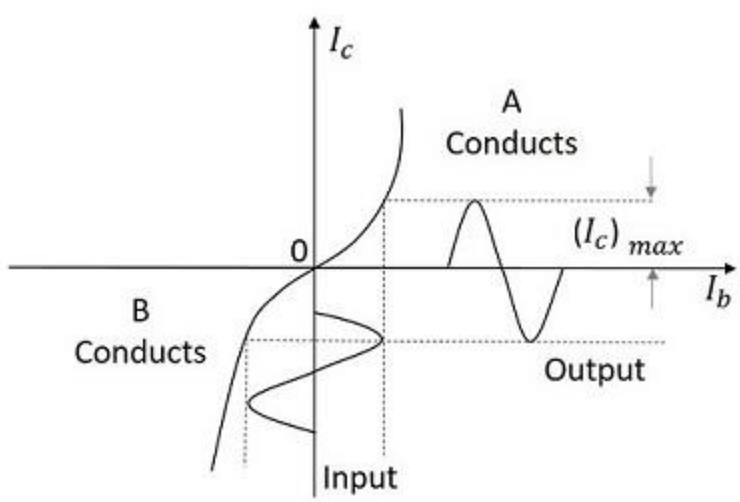
ADDITIONAL EXPERIMENTS

CIRCUIT DIAGRAM:

CLASS-B PUSHPULL POWER AMPLIFIER



MODFEL WAVEFORM:



Expt No: 01 **Date:**

CLASS-B PUSHPULL POWER AMPLIFIER

AIM: To design a class-B push-pull power amplifier in order to achieve maximum output AC power and efficiency.

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	Transistor	(BC107)	2
2	Resistors	15Ω	1
		100Ω	1
		6.2KΩ	1
		100Ω(Speaker)	
3	Zener Diode	IN4730A	1
4	RPS	0-30V	1
5	Function Generator	0-3MHz	1
6	CRO	0-30MHz	1
7	Bread board	-	1
8	Connecting wires	-	As Per Required

OPERATION:

The circuit arrangement of the Class B push pull amplifier is similar to the Class A push pull amplifier except for the absence of the biasing resistors. T1 is the input coupling capacitor and the input signal is applied to its primary. Q1 and Q2 are two identical transistors and their emitter terminals are connected together. Center tap of the input coupling transformer and the negative end of the voltage source is connected to the junction point of the emitter terminals. Positive end of the voltage source is connected to the center tap of the output coupling transformer. Collector terminals of each transistor are connected to the respective ends of the primary of the output coupling transformer T2. Load RL is connected across the secondary of T2.

The input signal is converted into two similar but phase opposite signals by the input transformer T1. One out of these two signals is applied to the base of the upper transistor while the other one is applied to the base of the other transistor. You can understand this from the circuit diagram.

When transistor Q1 is driven to the positive side using the positive half of its input signal, the reverse happens in the transistor Q2. That means when the collector current of Q1 is going in the increasing direction, the collector current of Q2 goes in the decreasing direction. Anyway the current flow through the respective halves of the primary of the T2 will be in same direction. Have a look at the figure for better understanding. This current flow through the T2 primary results in a wave form induced across its secondary. The wave form induced across the secondary is similar to the original input signal but amplified in terms of magnitude.

PROCEDURE:

1. Connect the circuit diagram as shown in the figure.

2. Determine the maximum signal handling capacity of the push pull amplifier.

3. Apply sinusoidal signal of 1V peak to peak voltage at a frequency of 1 kHz.

4. Connect the loud speaker at the output. If you hear sound note the circuit is working .Now replace the loud speaker with the Power meter at the O/P . Select the typical value of the load impedance in the power meter. Also connect the output to a CRO. See the wave shape of the output voltage on the CRO. Increase the input signal voltage till the output wave shape starts getting distorted. Note this input signal voltage . now reduce the input signal to a value slightly below this voltage.

5. By changing the load impedance note down the value of impedance and output Power meter.

6. Tabulate the readings.

7. Plot the graph between output Power and load impedance.

8. Select the load impedance is equal to the optimum load. See the Wave shape of the output on the CRO. Increase the input signal till the wave shape shows distortion and note down the input voltage. This gives the maximum signal handling capacity of the amplifier.

OBSERVATION:

VCC =12V

RL =100Ω

EFFICIENCY: $P_{ac}/P_{DC} = V_{mx}$ II /4 X $V_{CC} =$

Vm = Vpp/2

V_S=20mV

Input power, Pin=2VccIm/Π

Output power, Pout=VmIm/2

Power Gain or efficiency, $\eta = \pi/4(V_m / V_{cc})\ 100$

OBSERVATIONS: V_S=20mV

S.NO	RL	Output Power in db P_o (mW) (10 log P_0)	Power in db (10 log P0)

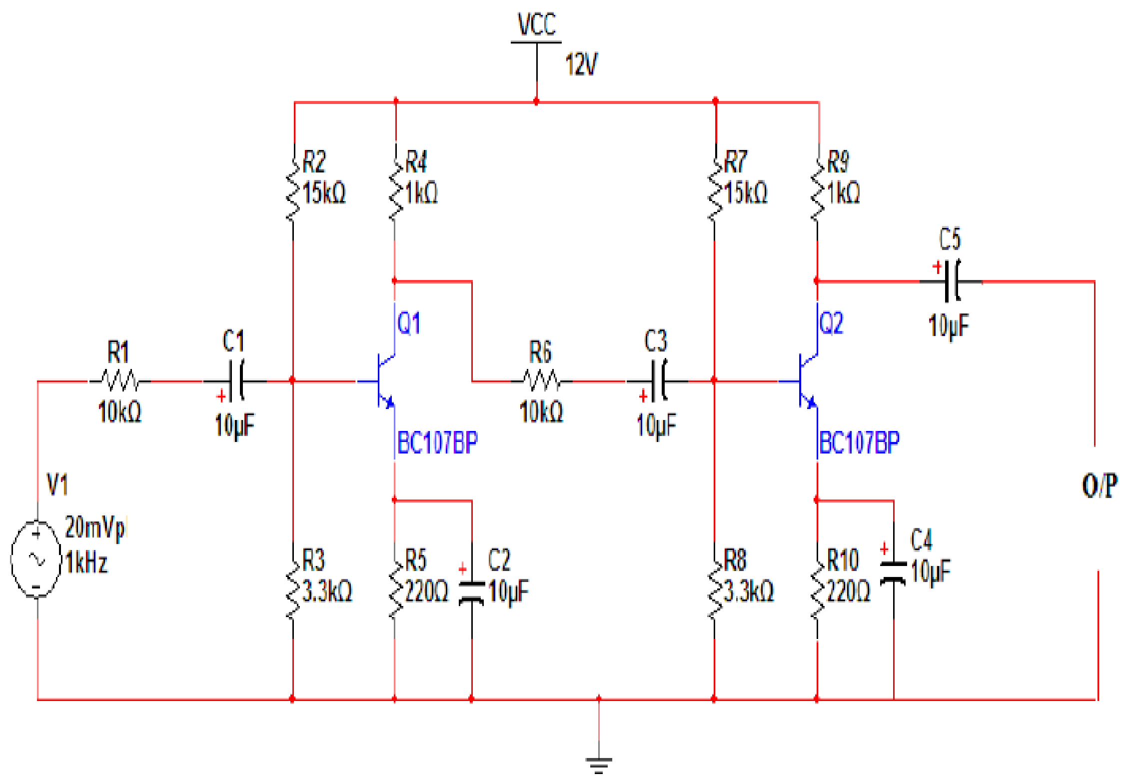
RESULT:

CONCLUSION:

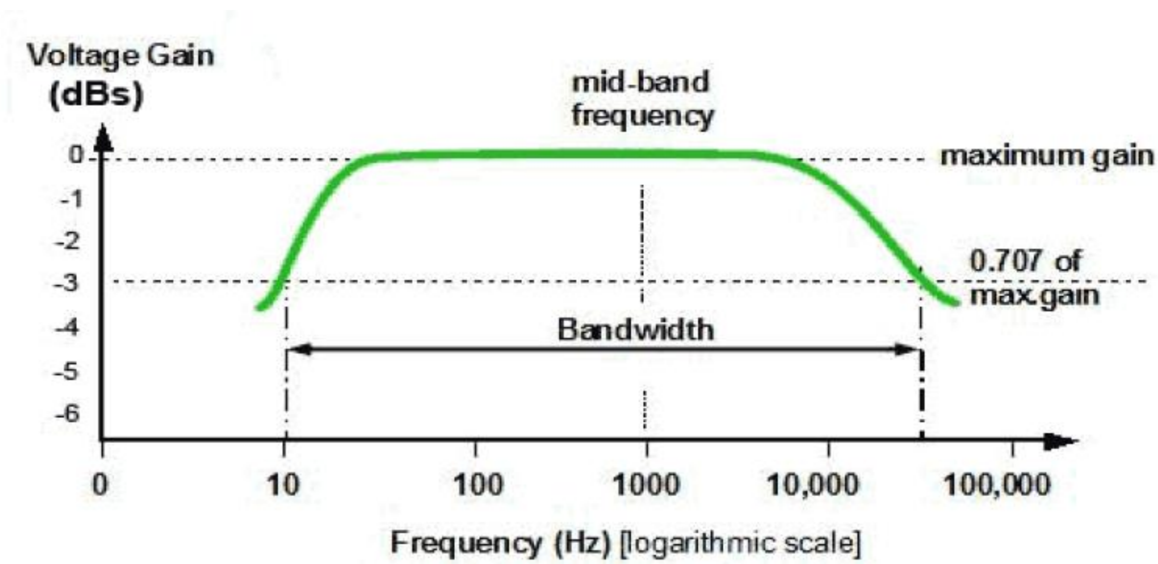
VIVA QUESTIONS:

1. What is the conduction angle of push pull amplifier?
2. What is the power efficiency of push pull amplifier?
3. What is crossover distortion?
4. What is operating point in push pull amplifier?
5. What are the advantages & disadvantages of class B Push Pull Amplifier?

CIRCUIT DIAGRAM:
CASCADE AMPLIFIER:



MODEL WAVEFORM:



Expt No: 02 **Date:**

CASCADE AMPLIFIER

AIM: To obtain the Voltage gain for Cascade Amplifier and also to observe the frequency Response.

APPARATUS:

S.NO	APPARATUS	RANGE	QUANTITY
1	Transistor	(BC107 or BC547)	2
2	Resistors	10 KΩ	2
		15K Ω	2
		1 KΩ	2
		3.3KΩ	2
		220Ω	2
3	Capacitors	10µF	5
4	RPS	0-12V	1
5	Function Generator	0-3MHz	1
6	CRO	30MHz	1
7	Bread board	-	1
8	Connecting wires	-	As Per Required

PROCEDURE:

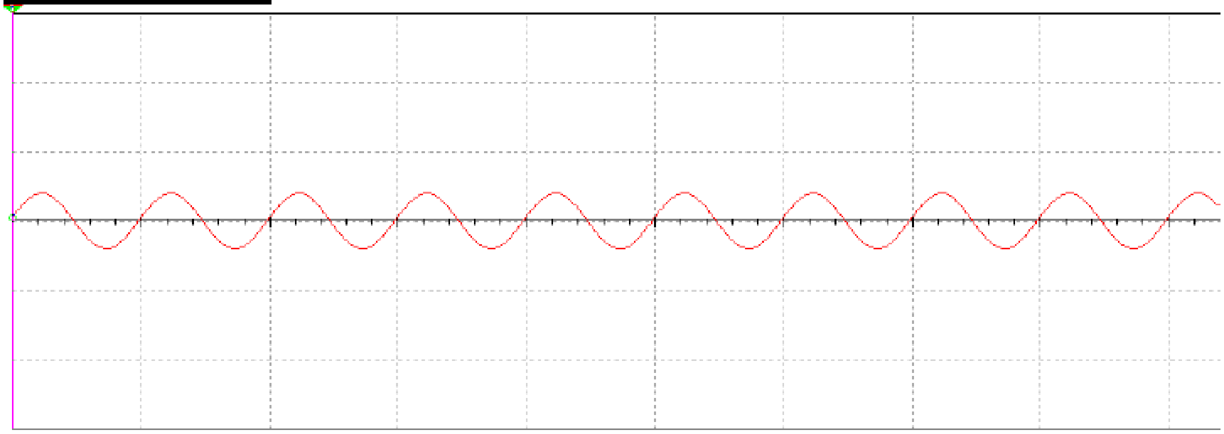
1) Connect the circuit as shown in the figure.
2) Apply 1Khz frequency and 20mv Vp-p Sine wave from function generator..
3) Observe input and output Waveforms simultaneously on C.R.O
4) Change the frequency of input signal from 10HZ to 1MHZ in steps and note amplitudes of input and output Waveforms(input signal should be maintained constant).
5) Calculate Voltage gain (A) for each (in db) verses frequency.

PRECAUTIONS:

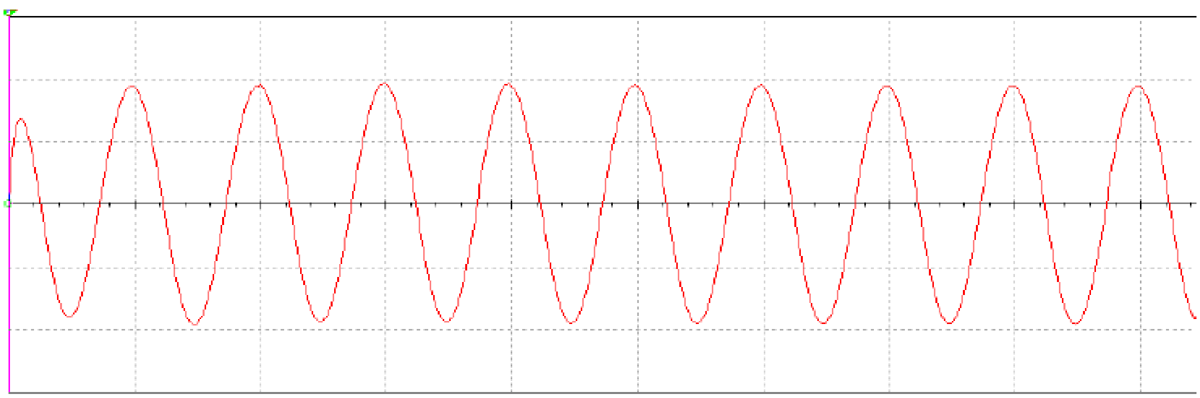
Avoid loose connections give proper input voltage

MODEL GRAPH:

Input wave form



Output waveform



OBSERVATIONS: V_S=20mV

S.NO	FREQUENCY(Hz)	OUTPUT VOLTAGE (V)	GAIN (V_0/V_i)	GAIN IN dB $A_v=20\log_{10}(V_0/V_i)$

CALCULATION:

Maximum gain of the amp:

Upper cutoff frequency F2:

Lower cutoff frequency F1:

Band width=F2-F1

RESULT:

CONCLUSION:

VIVA QUESTIONS:

1. What is a cascaded amplifier?

2. What is the voltage gain of cascade amplifier?

3. What is Current gain of cascade amplifier?

4. What is the input and output impedance of Cascade Amplifier?

5. What is the need of Cascade Amplifier?